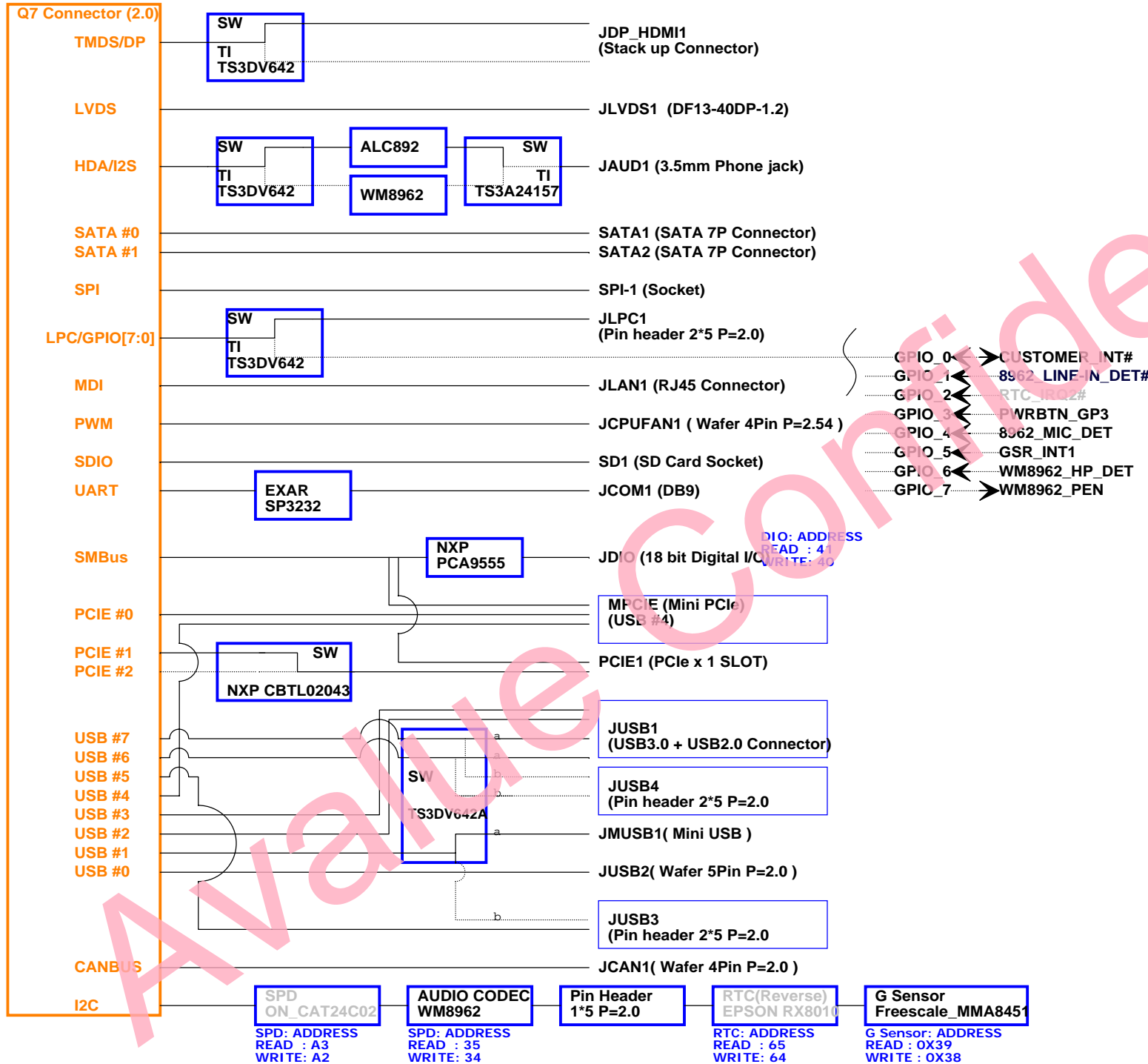


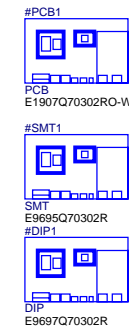
# REV-Q703 A1 Block diagram

QSeven 2.0 Carrier Board



## Cover Sheet:

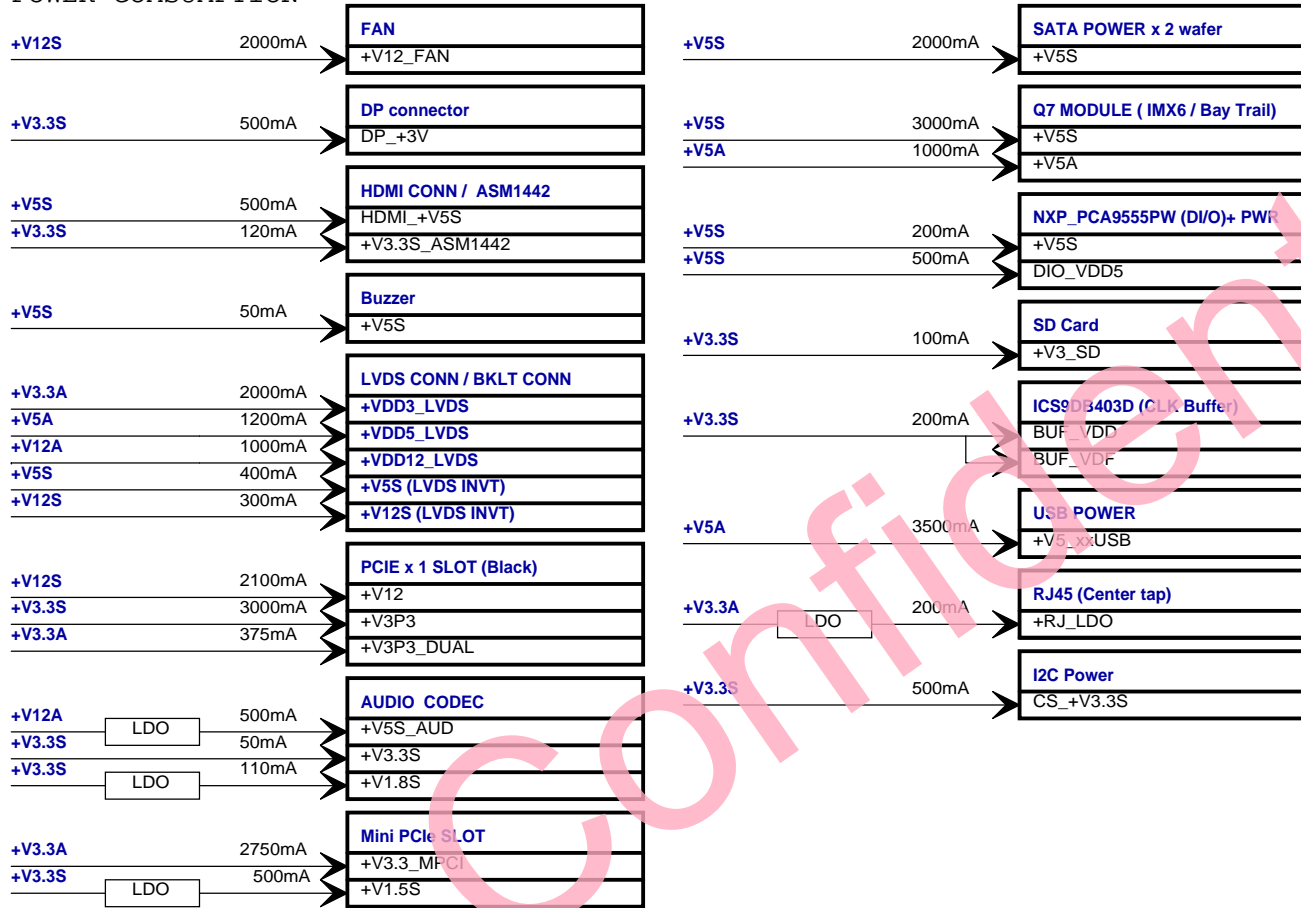
- 01.Cover Sheet / Block Diagram
- 02.Power Delivert Map,Reset Map
- 03.Power on squence
- 04.DP\_TMD5\_SWITCH / FUNC SEL
- 05.DP CONN
- 06.HDMI CONN
- 07.LVDS CONN
- 08.SATA/SP/DIO/SD/SPD
- 09.PCIE CLOCK BUFFER / COM PORT
- 10.MINI PCIE SLOT/ +V1.5S
- 11.PCIE x1 SLOT
- 12.USB 2.0 / 3.0 SW
- 13.USB 3.0 x1 / USB 2.0 x 6
- 14.RJ45 / Mini USB
- 15.Q7 Connector
- 16.Front Panel / WDT
- 17.LPC\_GPIO\_SWITCH
- 18.PWR OK / FAN / LPC / RTC
- 19.V12S,V5S,V3.3S/G Sensor/CAN
- 20.TPS51220A +V5A & +V3.3A
- 21.DC 12 Vin / Discharge
- 22.HDA & I2S Switch
- 23.AUDIO ALC892 / Buzzer
- 24 AUDIO WM8962
- 25.AUDIO PHONE JACK
- 26.History



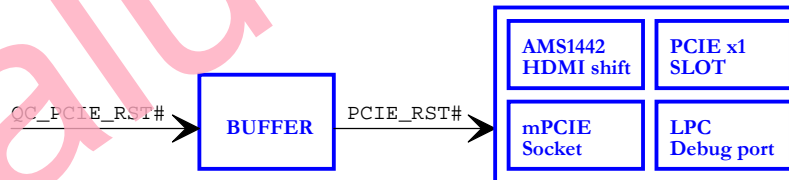
<b>avalue</b> Technology Inc.		<b>Confidential</b>	
Project Name	REV-Q703	Module Number	<Module no.> ?
Size	Custom	Title	Cover Sheet / Block Diagram
Date:	Friday, July 03, 2015	Sheet	1 of 26

# Power Delivery Map

## POWER CONSUMPTION



## RESET MAP



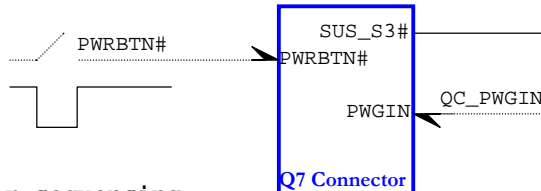
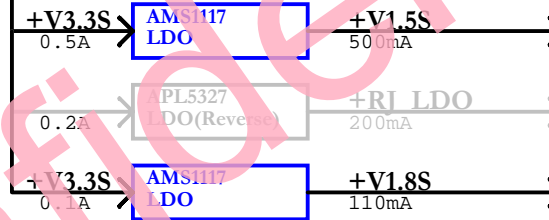
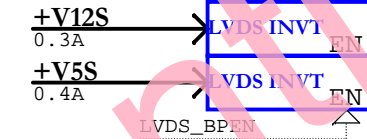
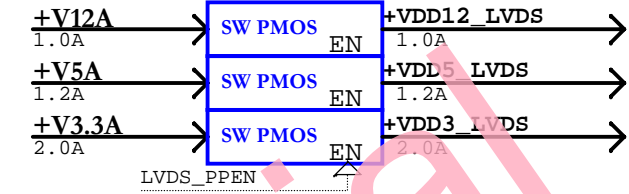
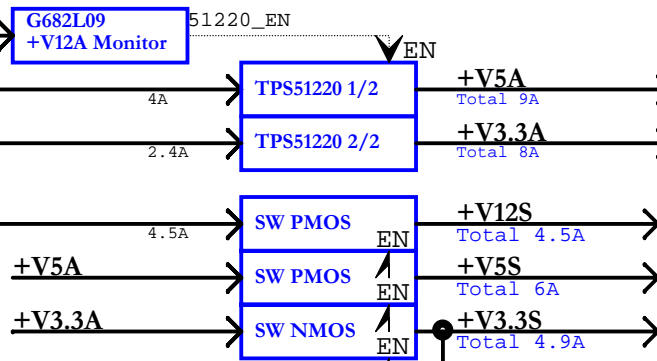
# Power on sequence

DC IN 12V  
12A



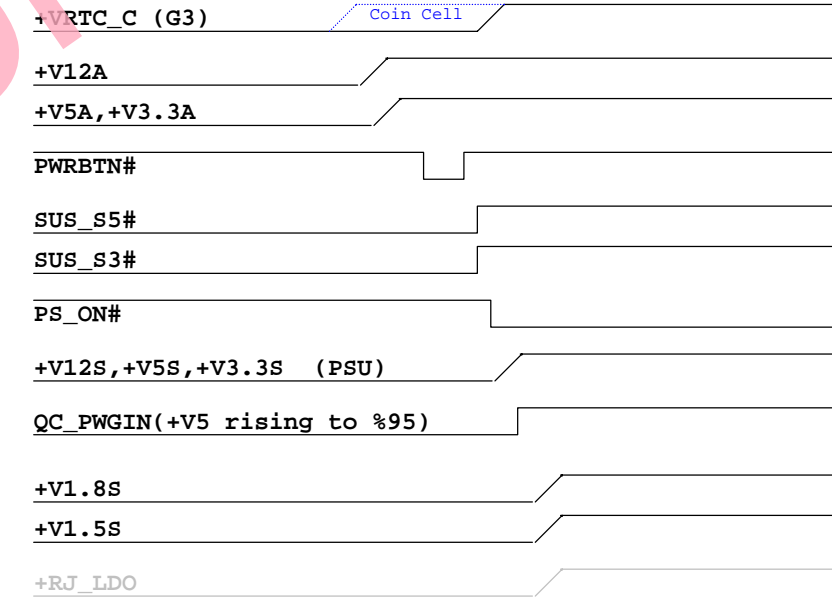
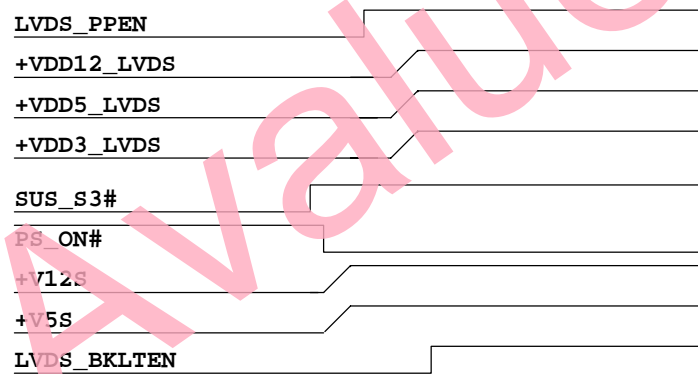
+V12A  
Total 11A

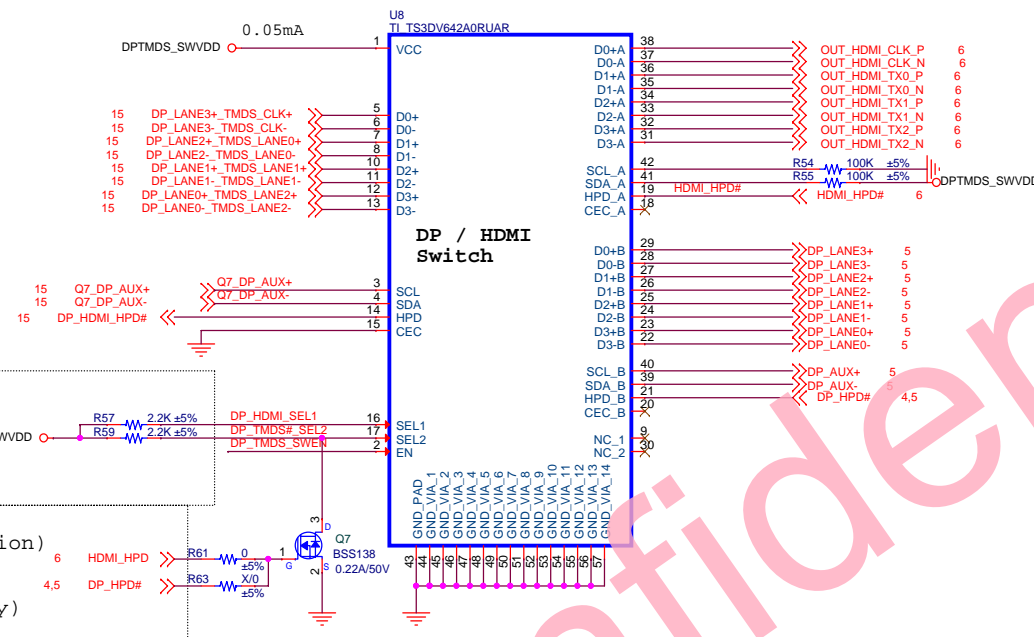
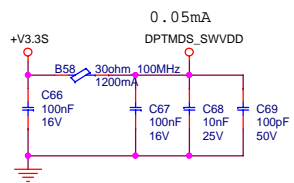
I LIM(min) is 9.7A  
I LIM(typ) is 11.1A  
I LIM(max) is 12.3A  
116.4W - 133.2W - 147.6W



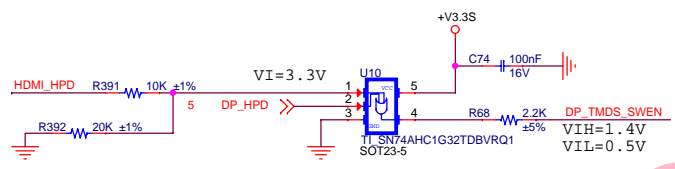
Qseven input power sequencing requirements are as follows:

- +VRTC rise to +V5A >=0ms
- +V5A rise to +V5S >=0ms
- +V5S VCC rise to 95% to PWGIN >=0ms





Pin17 input logic (Auto selection)  
 DP vs HDMI ,pin17 SEL2  
 HI , DP OUTPUT.  
 LOW, HDMI OUTPUT.(High Priority)



When insert HDMI or DP cable  
 switch IC enable.

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

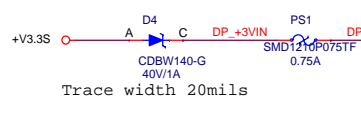
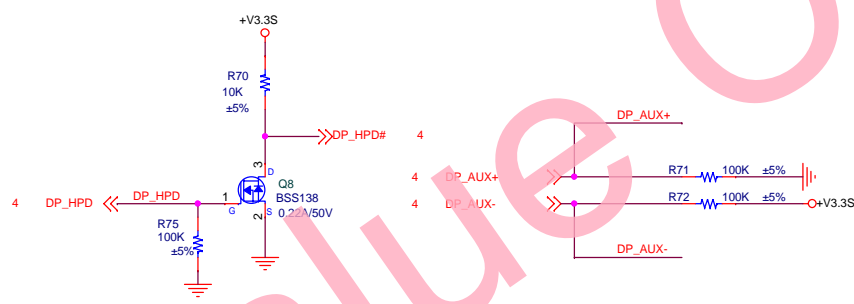
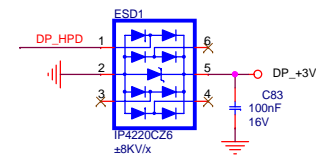
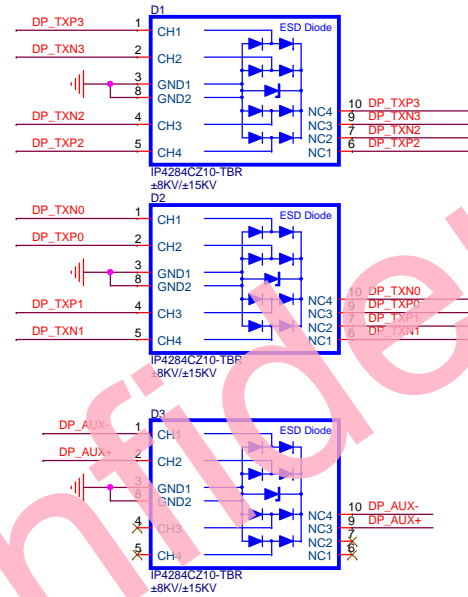
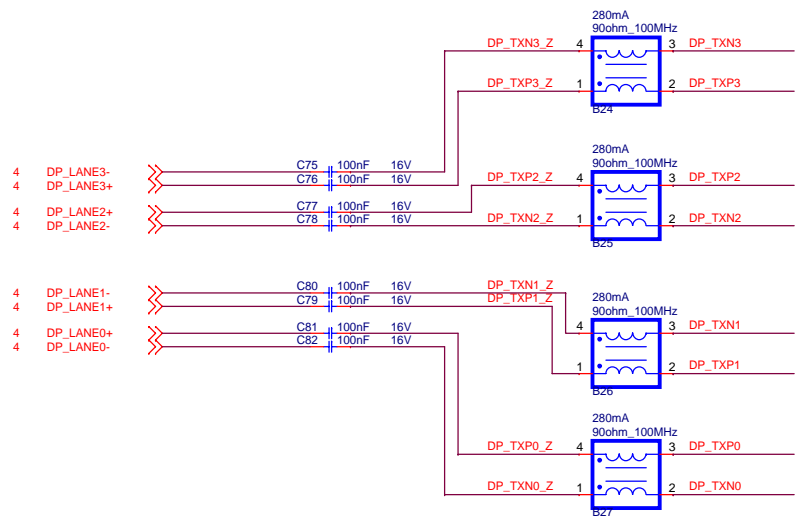
Use all channel.

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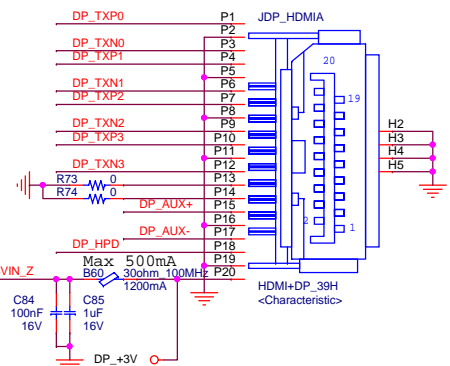
Project Name: **REV-Q703**      Module Number: **<Module no.>**      Rev: **?**

Size: **A3**      Title: **DP\_TMDS\_SWITCH**      Rev: **A1**

Date: **Friday, July 03, 2015**      Sheet: **4** of **26**

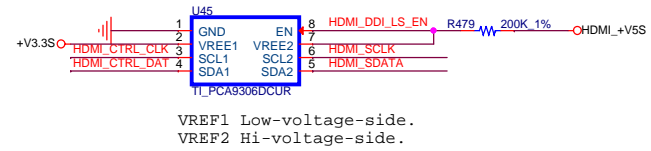
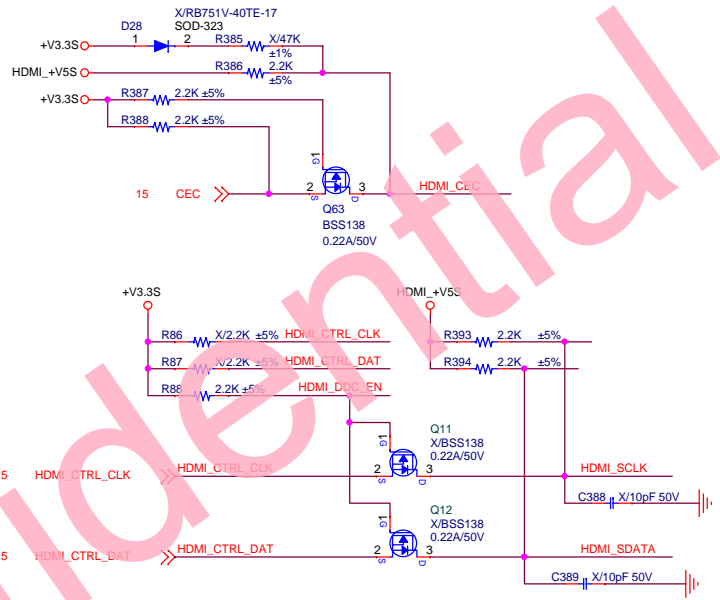
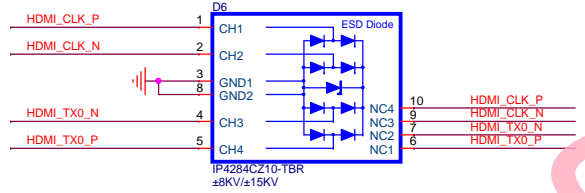
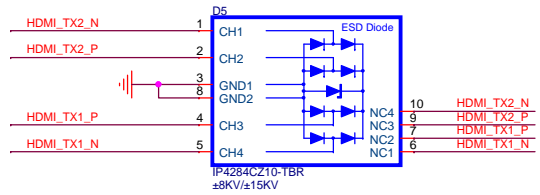
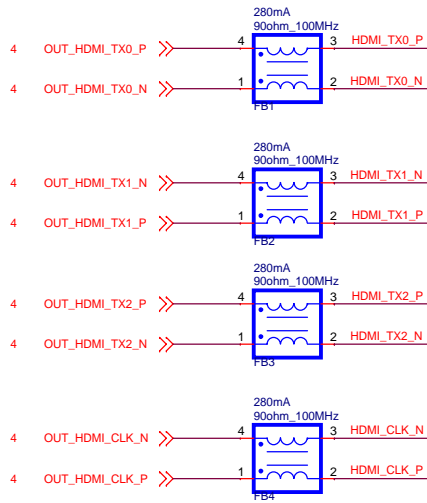


**DP CONN**

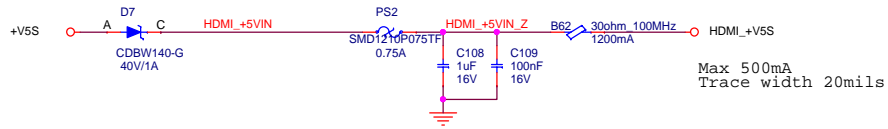
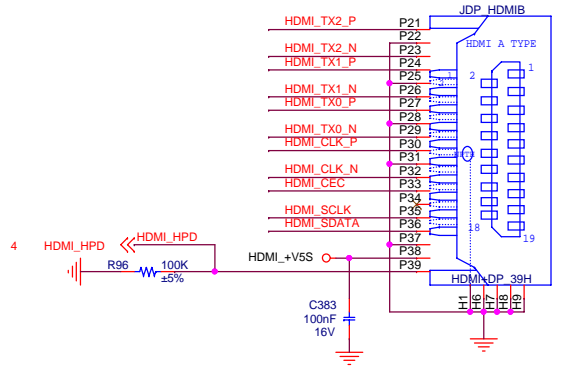
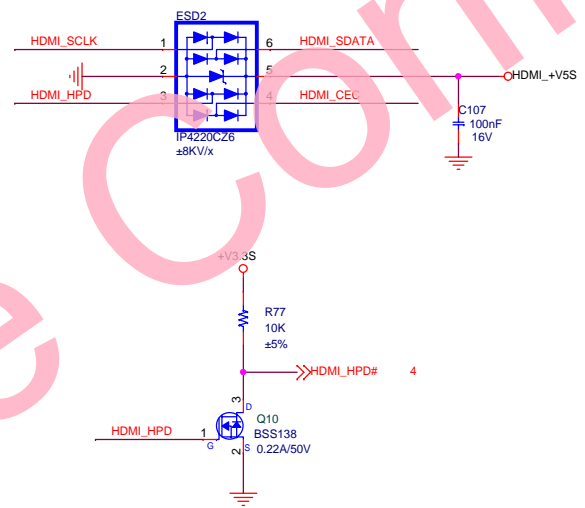
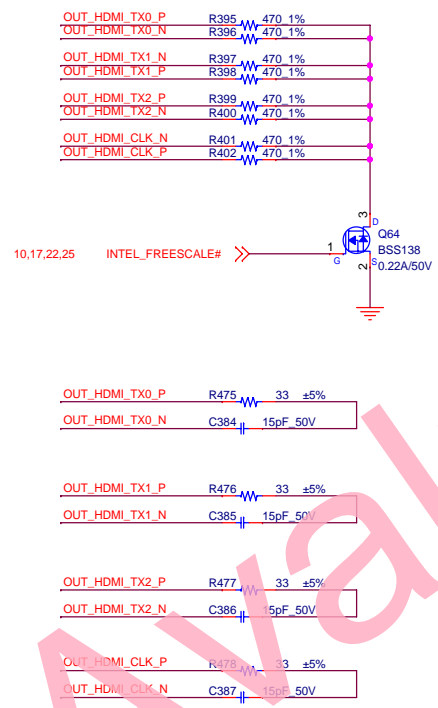


Available Confidential

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Project Name	REV-Q703	Module Number	<Module no.>
Size	A3	Title	DP Connector
Date:	Friday, July 03, 2015	Sheet	5 of 26



### HDMI CONN

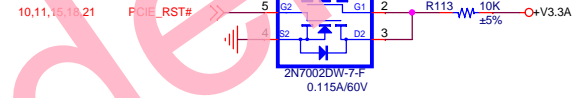
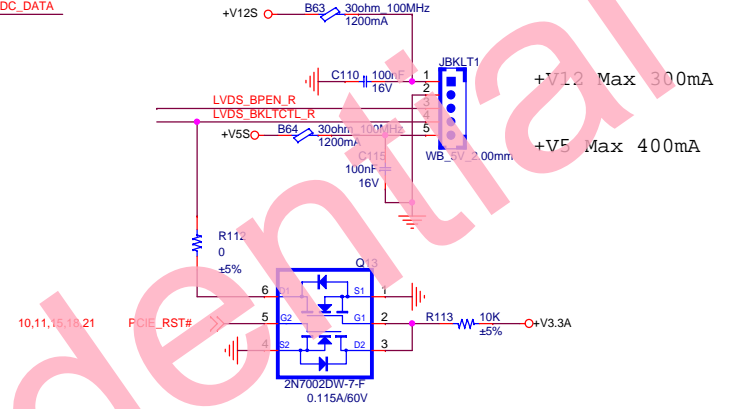
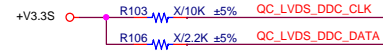
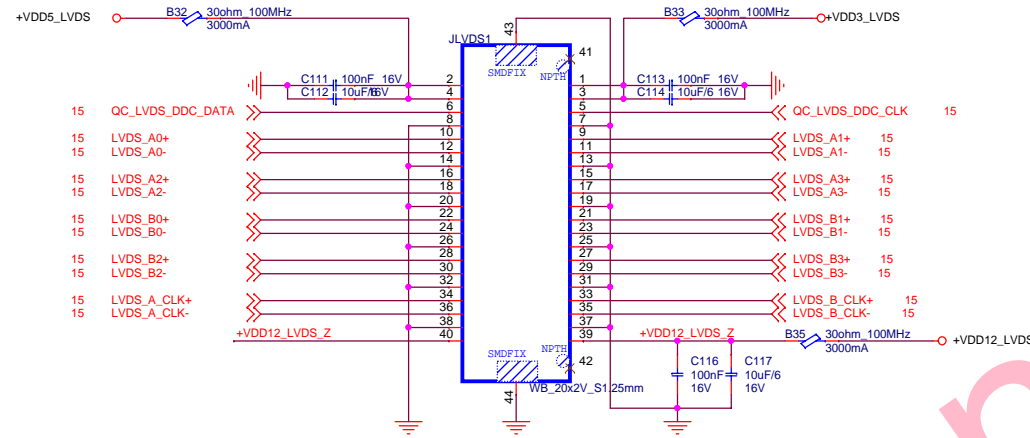


		<b>Confidential</b>	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title HDMI CONN	Date	Rev ?
Date	Friday, July 03, 2015	Sheet	6 of 26

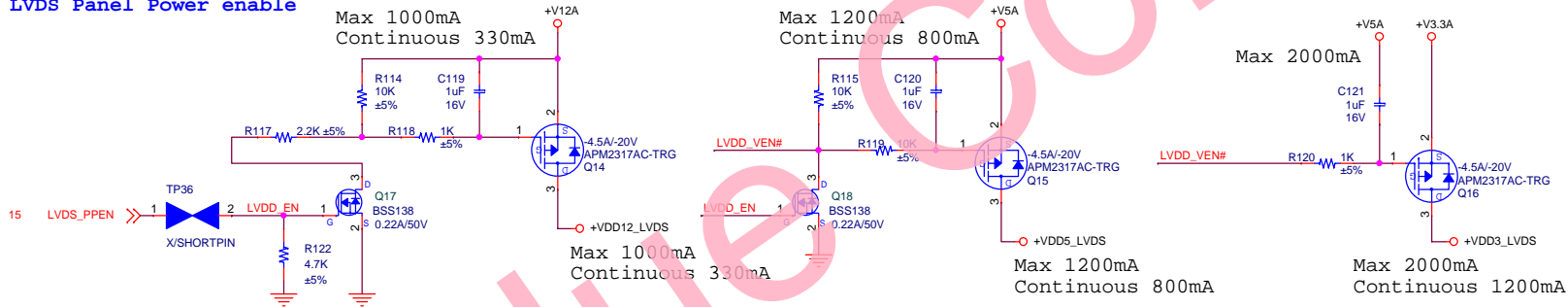
# LVDS CONN

**Near conn.**

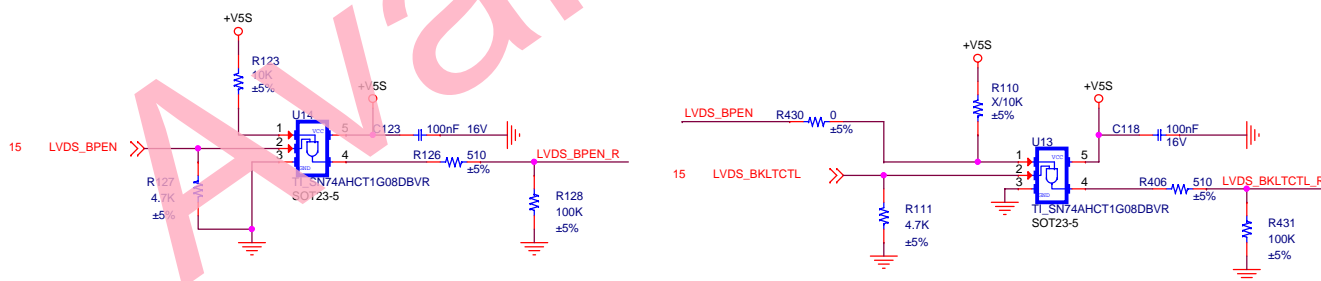
LVDS_A0+	R97	100 ±5%	LVDS_A0-
LVDS_A1+	R98	100 ±5%	LVDS_A1-
LVDS_A2+	R99	100 ±5%	LVDS_A2-
LVDS_A3+	R100	100 ±5%	LVDS_A3-
LVDS_B0+	R101	100 ±5%	LVDS_B0-
LVDS_B1+	R102	100 ±5%	LVDS_B1-
LVDS_B2+	R104	100 ±5%	LVDS_B2-
LVDS_B3+	R105	100 ±5%	LVDS_B3-
LVDS_A_CLK+	R107	100 ±5%	LVDS_A_CLK-
LVDS_B_CLK+	R108	100 ±5%	LVDS_B_CLK-



## LVDS Panel Power enable



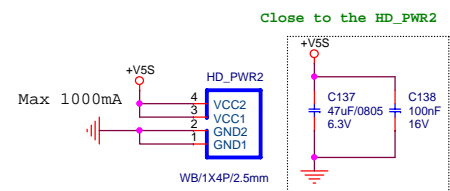
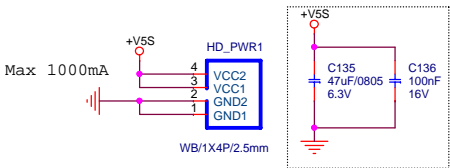
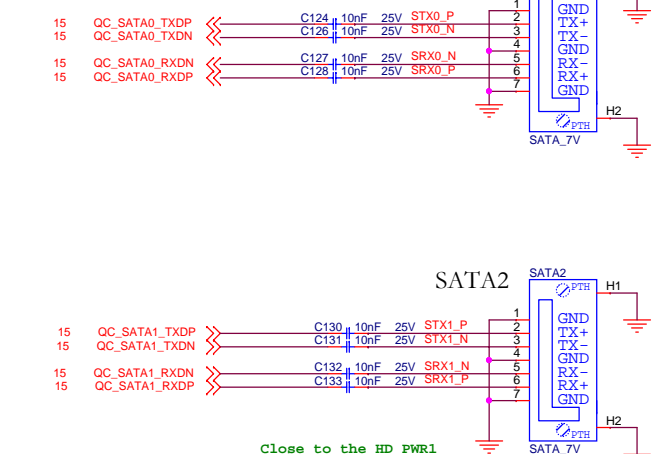
## Backlight Power enable



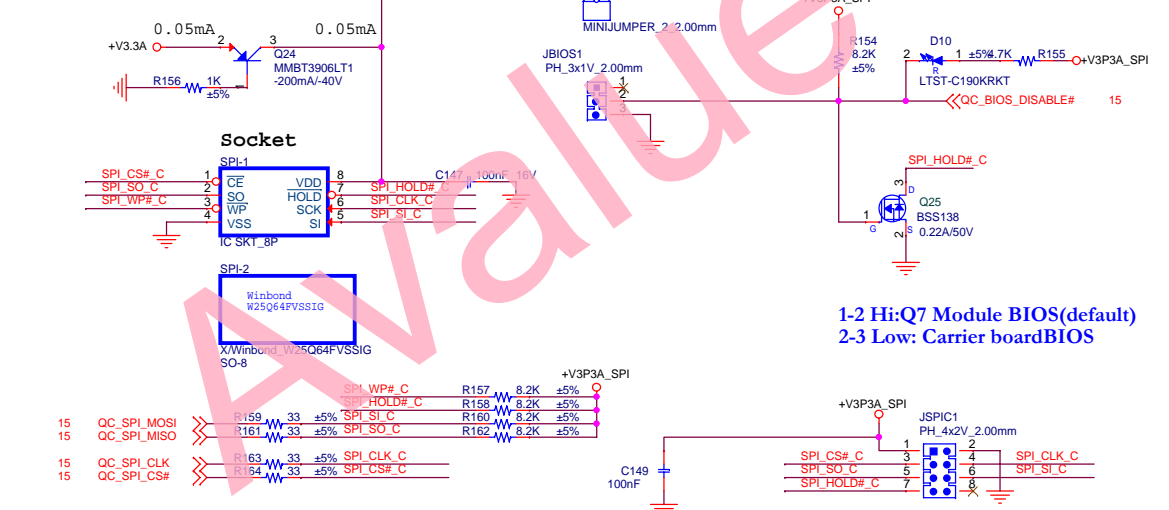
<b>avalue</b> Technology Inc.		<b>Confidential</b>	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title	LVDS Connector	Rev ?
Date:	Friday, July 03, 2015	Sheet	7 of 26



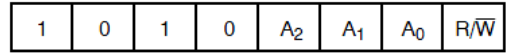
# SATA



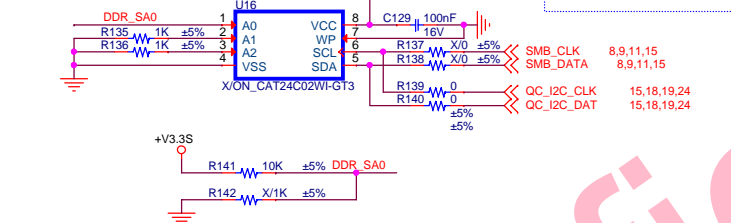
# SPI



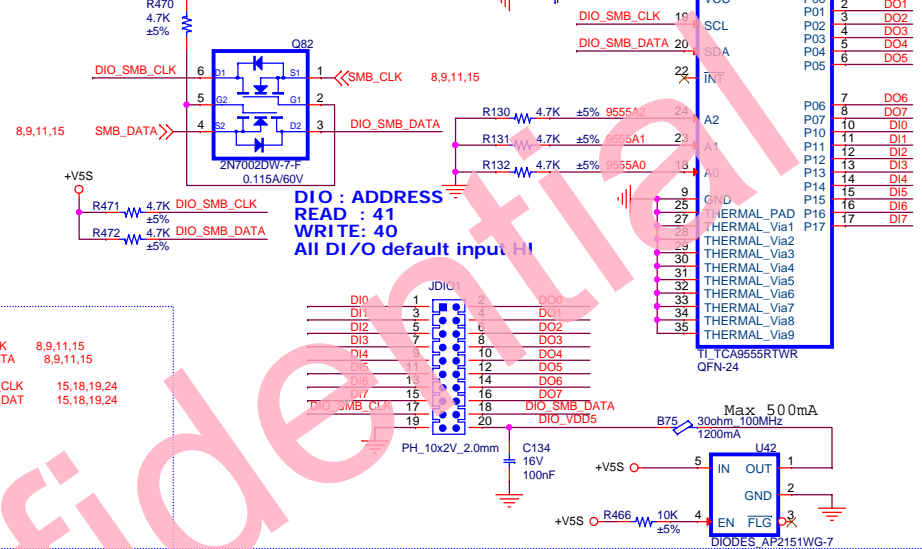
# SPD



DDR3 SPD: ADDRESS  
READ : A3  
WRITE : A2

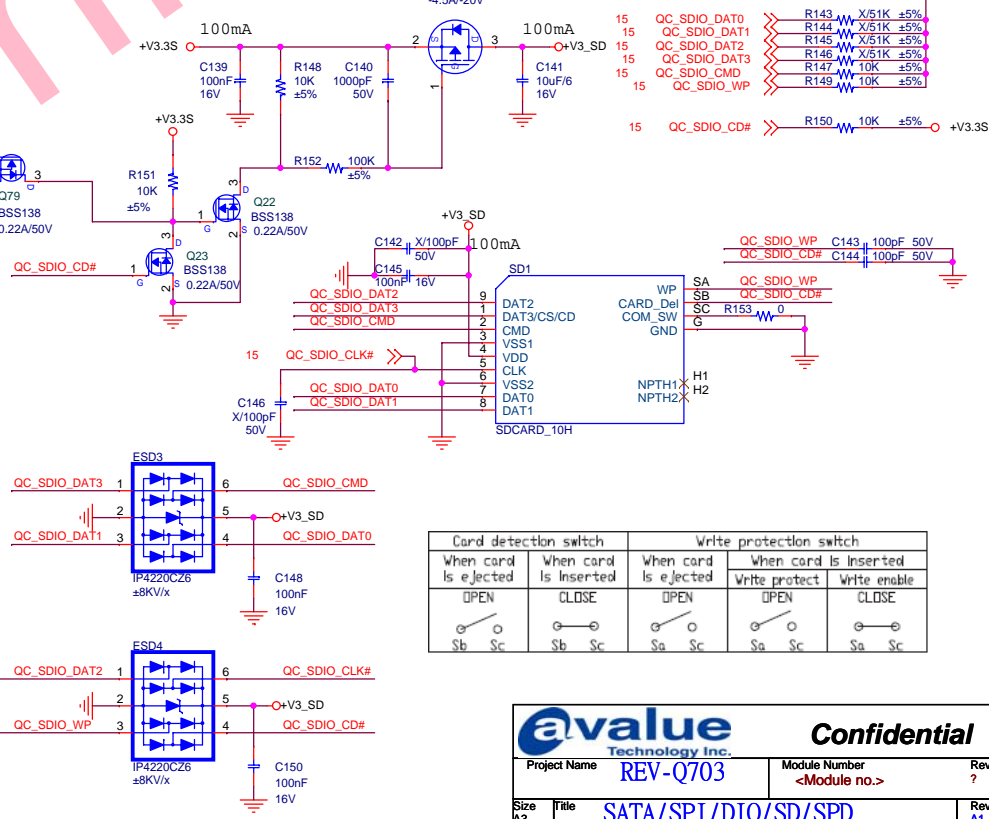


# DIO8\*8



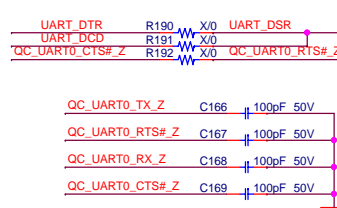
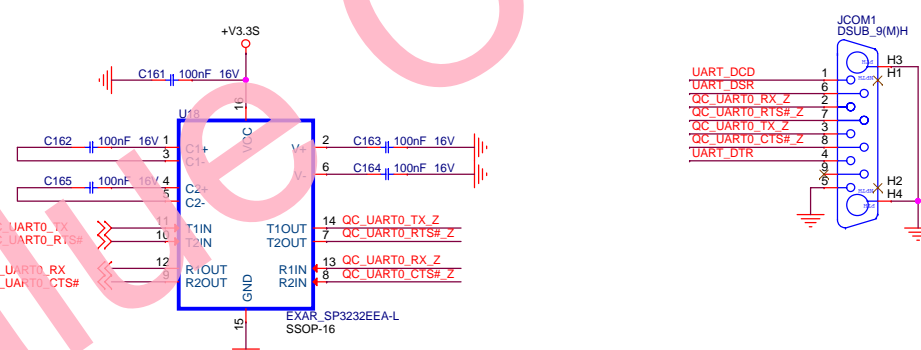
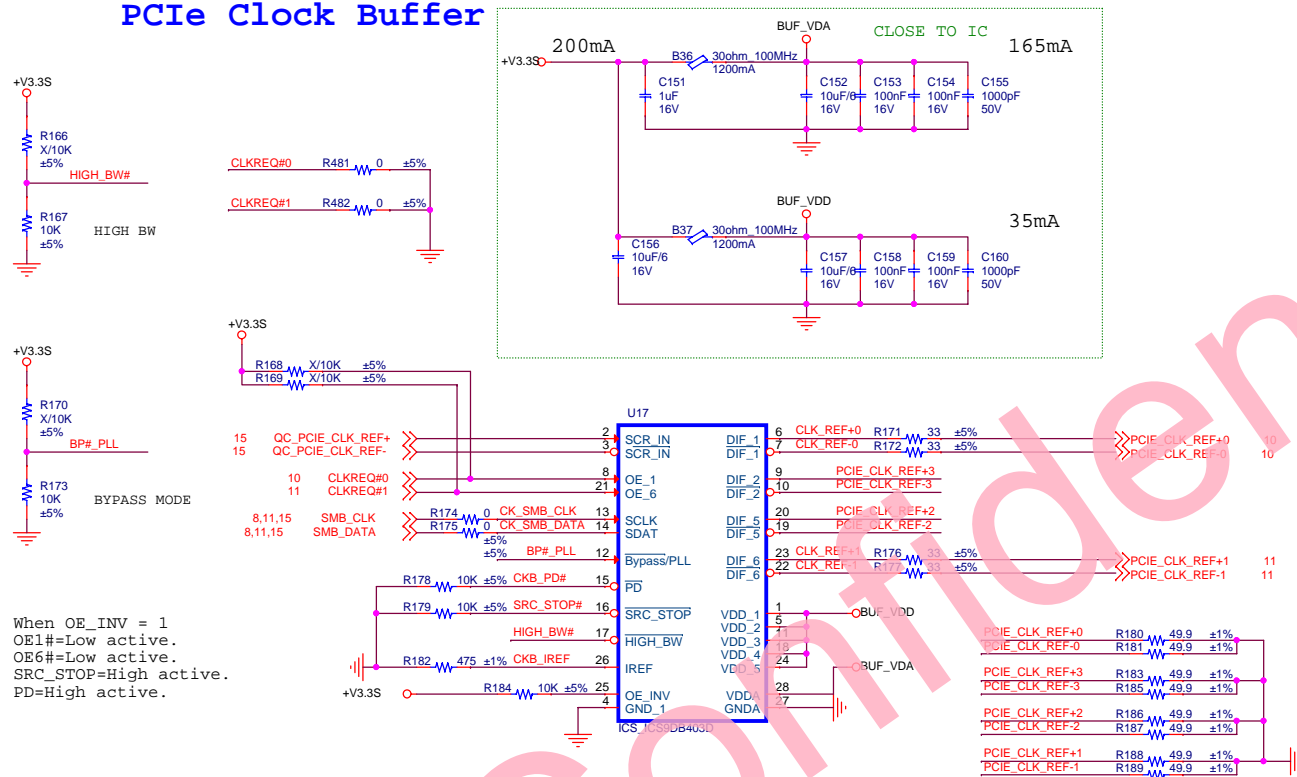
DIO : ADDRESS  
READ : 41  
WRITE : 40  
All DI/O default input HI

# SD CARD



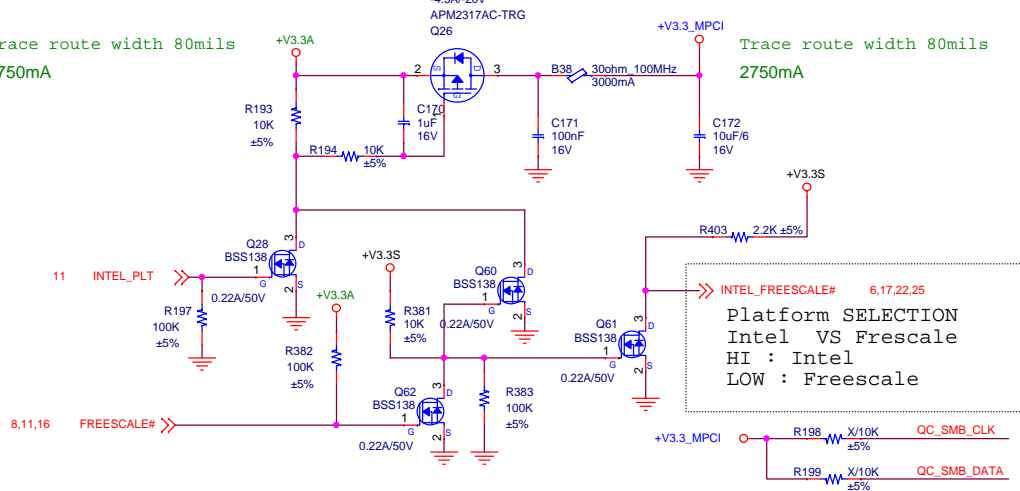


# PCIe Clock Buffer



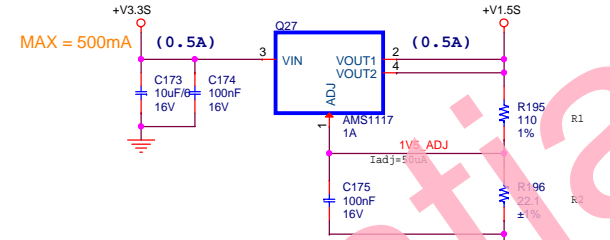
		<b>Confidential</b>	
		Project Name	Module Number
Size	Title	Rev	?
A3	PCIe CLOCK BUFFER / COM PORT	A1	
Date:	Friday, July 03, 2015	Sheet	9 of 26

Trace route width 80mils  
2750mA



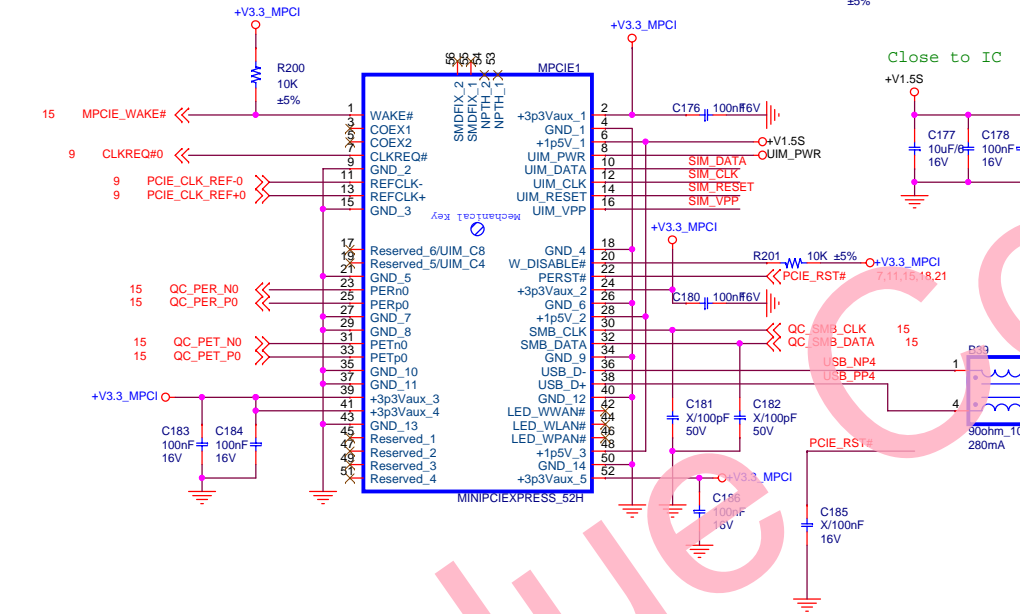
## +V1.5S Power

Trace route width 20mils

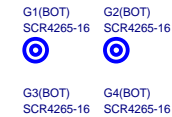
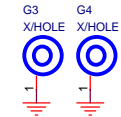
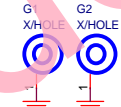


minimux load 10mA  
 $V_{OUT} = V_{REF} (1 + R2/R1) + I_{ADJ} R2$   
 $= 1.25 * [1 + (R2/R1)] + 50\mu A * R2$

LDO: +V3.3S to +V1.5S - 500mA



Close to IC

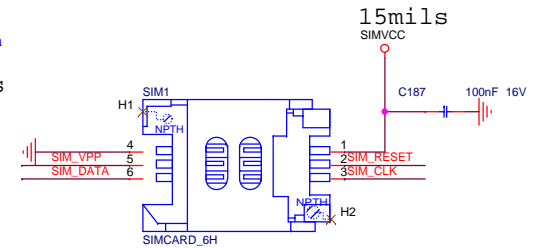
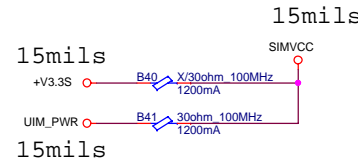


G3(TOP)  
F/M M2\*4.35/M3\*3mm

G4(TOP)  
F/M M2\*4.35/M3\*3mm

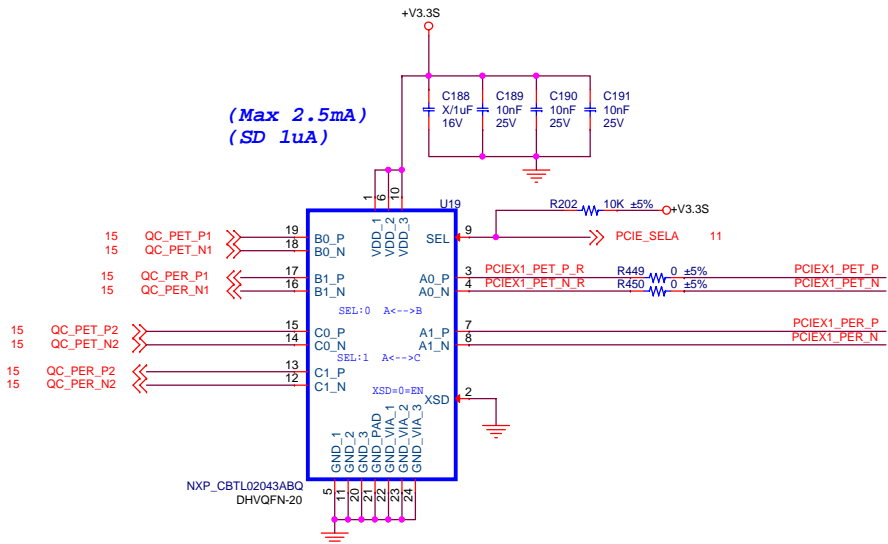
Power Rail	Voltage Tolerance	D0-D2, D3 <sup>hot</sup> Power <sup>1</sup>		D3 <sup>cold</sup> Power <sup>2,3</sup>	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	±9%	2,750	1,100	2,750 (wake enabled)	250 (wake enabled)
+1.5V	±5%	500	375	N/A	N/A

## SIM Card Push Push



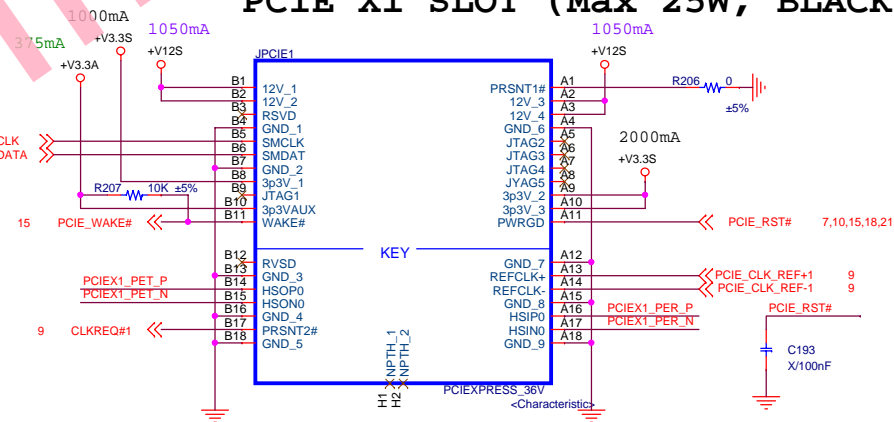
# PCIE PORT SWITCH

(Max 2.5mA)  
(SD 1uA)



SEL	9	12	CMOS single-ended input	operation mode select SEL = LOW: A ↔ B SEL = HIGH: A ↔ C
XSD	2	19	CMOS single-ended input	Shutdown pin; should be driven LOW or connected to V <sub>SS</sub> for normal operation. When HIGH, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized.

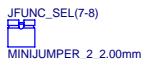
# PCIE X1 SLOT (Max 25W, BLACK)



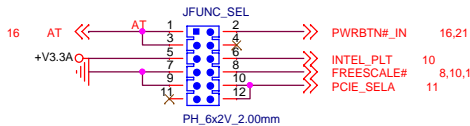
**AT and ATX Mode SELECTION**  
AT mode VS ATX mode  
SHORT 1-2 : For AT mode (default); OPEN 3-4  
SHORT 3-4 : For ATX mode; OPEN 1-2



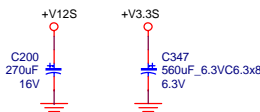
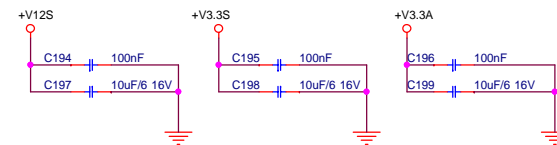
**Platform SELECTION**  
Intel VS Freescale  
SHORT 5-6 : For Intel platform; OPEN 7-8  
SHORT 7-8 : For Freescale platform(default) OPEN 5-6



**PCIe channel selection**  
PCIe1 VS PCIe2  
SHORT 9-10 : For PCIe1 (default); OPEN 11-12  
SHORT 11-12 : For PCIe2; OPEN 9-10



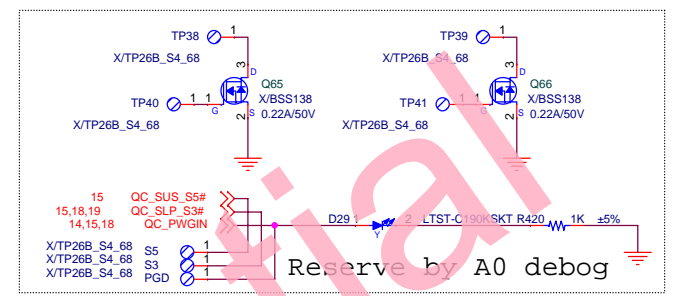
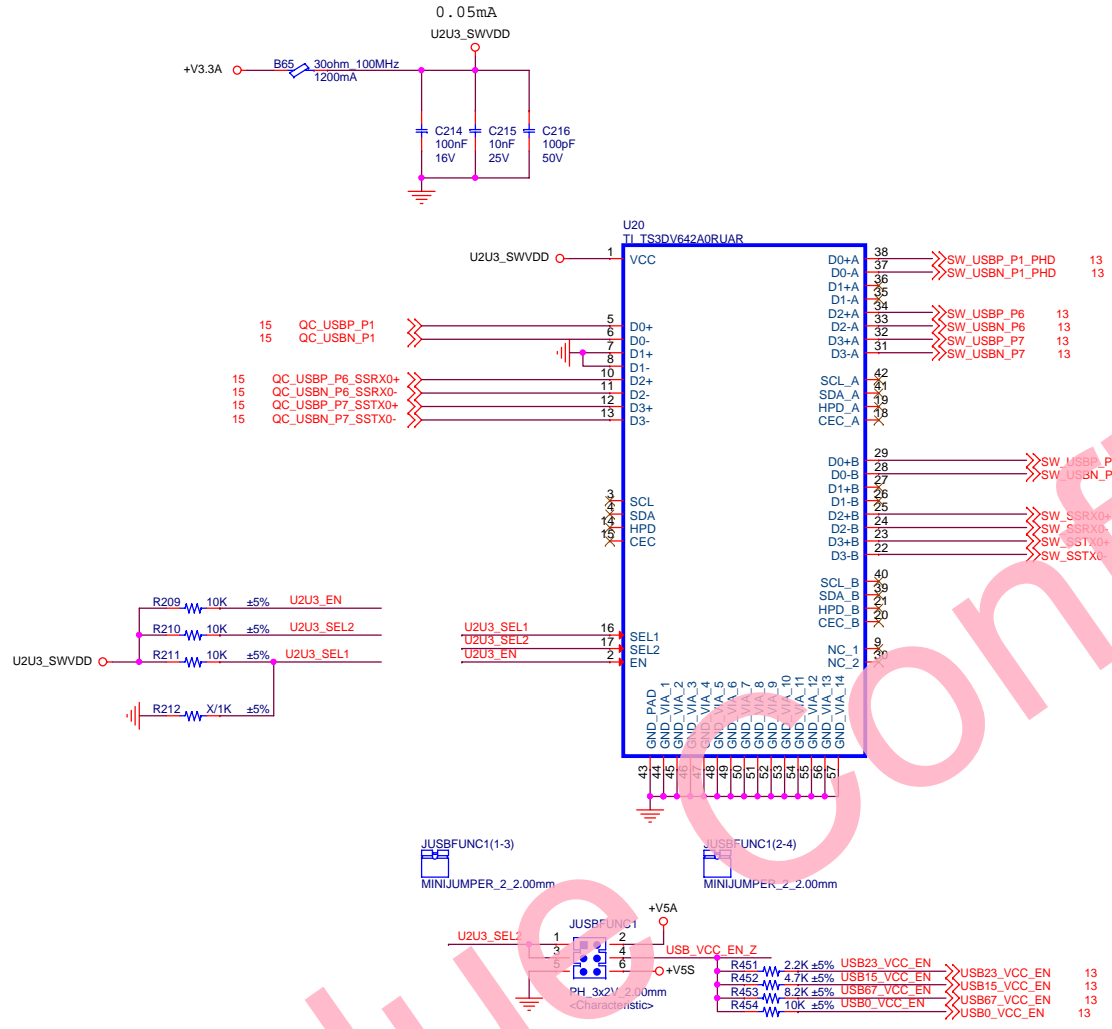
## Closed to Connector



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Project Name	REV-Q703	Module Number	<Module no.>	Rev	?
Size	A3	Title	PCIe x1 SLOT/ FUNC SEL	Rev	A1
Date:	Friday, July 03, 2015	Sheet	11	of	26

# USB 2.0 / 3.0 Switch



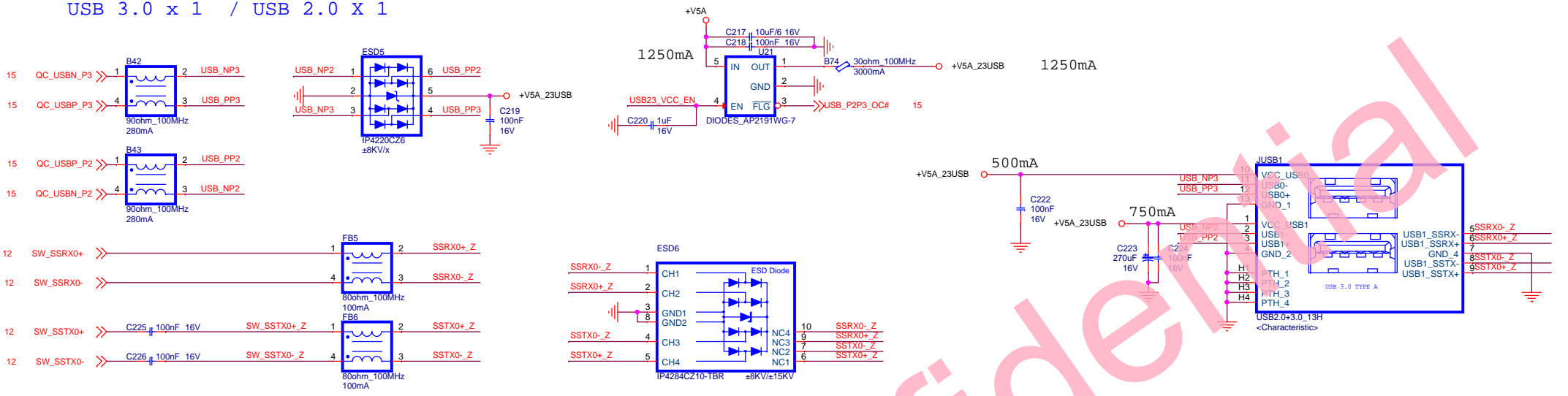
**JUSBFUNC1 SELECTION**  
**SHORT1-3:** Port 1,6,7 to B(Mini USB & USB3.0 CONN, default ). Used JMUSB1 & JUSB1(USB3.0) or  
**SHORT3-5:** Port 1,6,7 to A(USB 2.0 x1 & USB 2.0 x1 pin header) . Used JUSB3 & JUSB4  
**SHORT 2-4 :** It provided standby power to USB. (default)  
**SHORT 4-6 :** It provided USB power when main power ok.

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

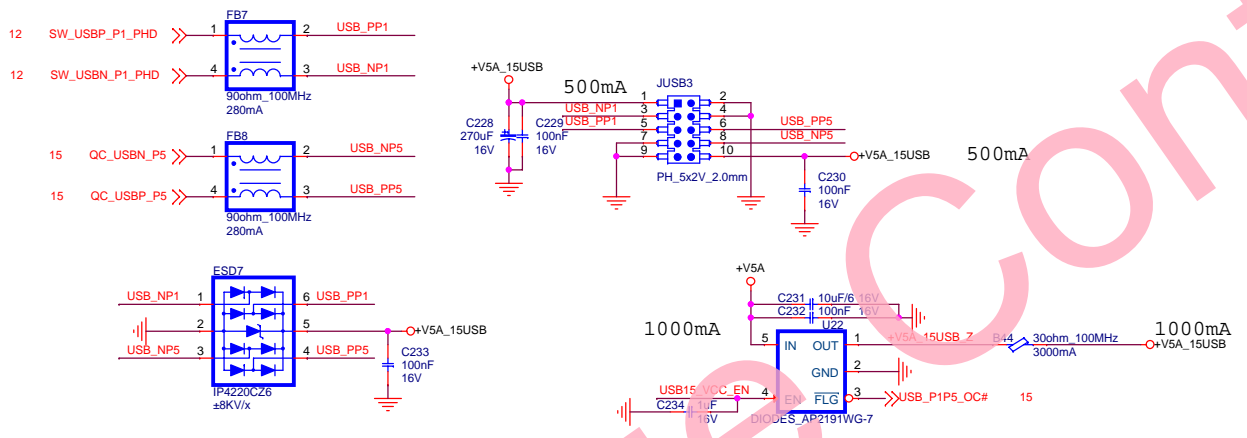
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Project Name	REV-Q703	Module Number	<Module no.>	Rev	?
Size	A3	Title	USB 2.0 / 3.0 SWITCH	Rev	A1
Date:	Friday, July 03, 2015	Sheet	12	of	26

USB 3.0 x 1 / USB 2.0 X 1



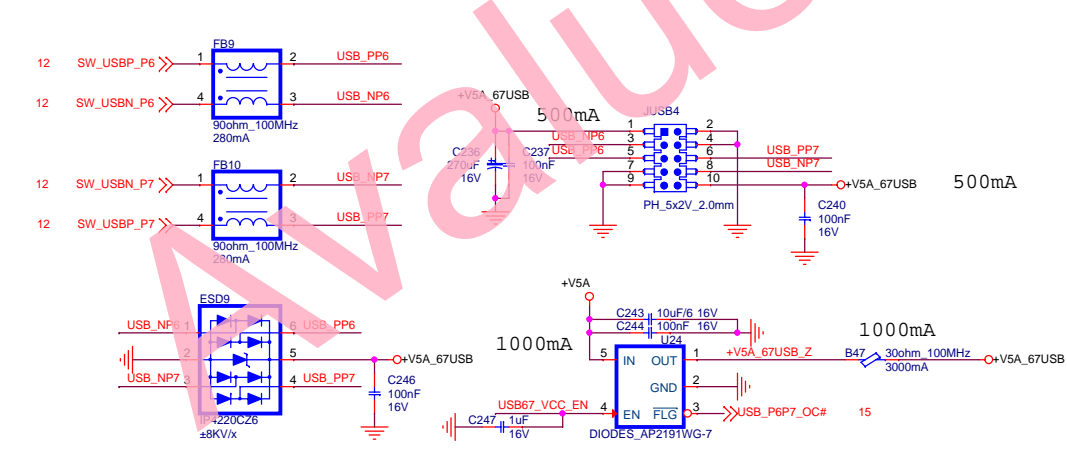
USB 2.0 x 2



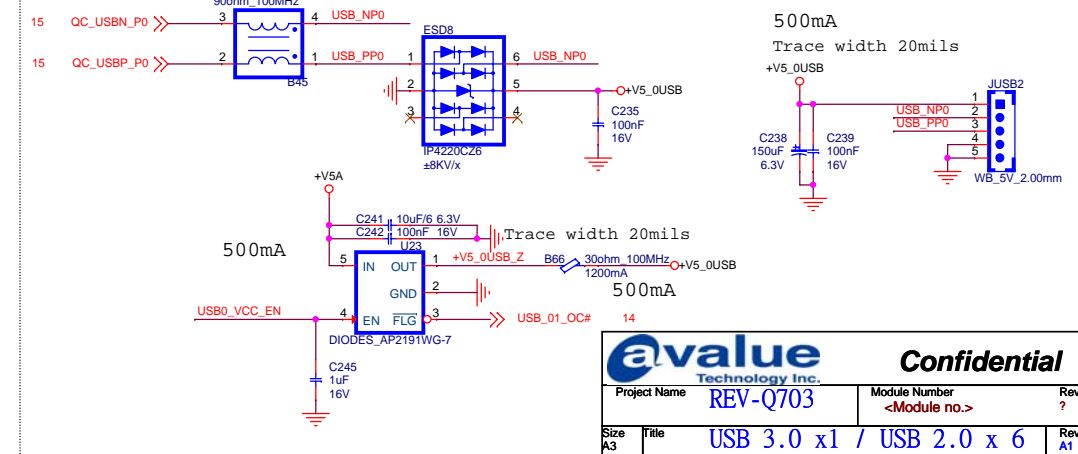
USB Power EN

- 12 USB23\_VCC\_EN >>> USB23\_VCC\_EN
- 12 USB15\_VCC\_EN >>> USB15\_VCC\_EN
- 12 USB67\_VCC\_EN >>> USB67\_VCC\_EN
- 12 USB0\_VCC\_EN >>> USB0\_VCC\_EN

USB 2.0 x 2



USB 2.0 x 1 (FOR TOUCH FUNCTION)

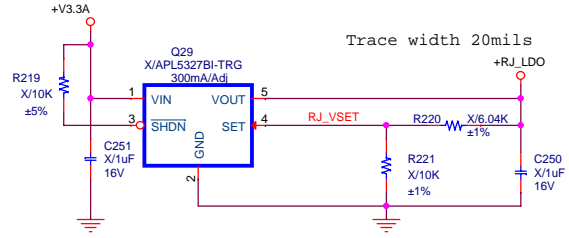


**a value** Technology Inc. **Confidential**

Project Name	REV-Q703	Module Number	<Module no.>	Rev ?
Size A3	Title	USB 3.0 x1 / USB 2.0 x 6		Rev A1
Date:	Friday, July 03, 2015	Sheet	13	of 26

# RJ45

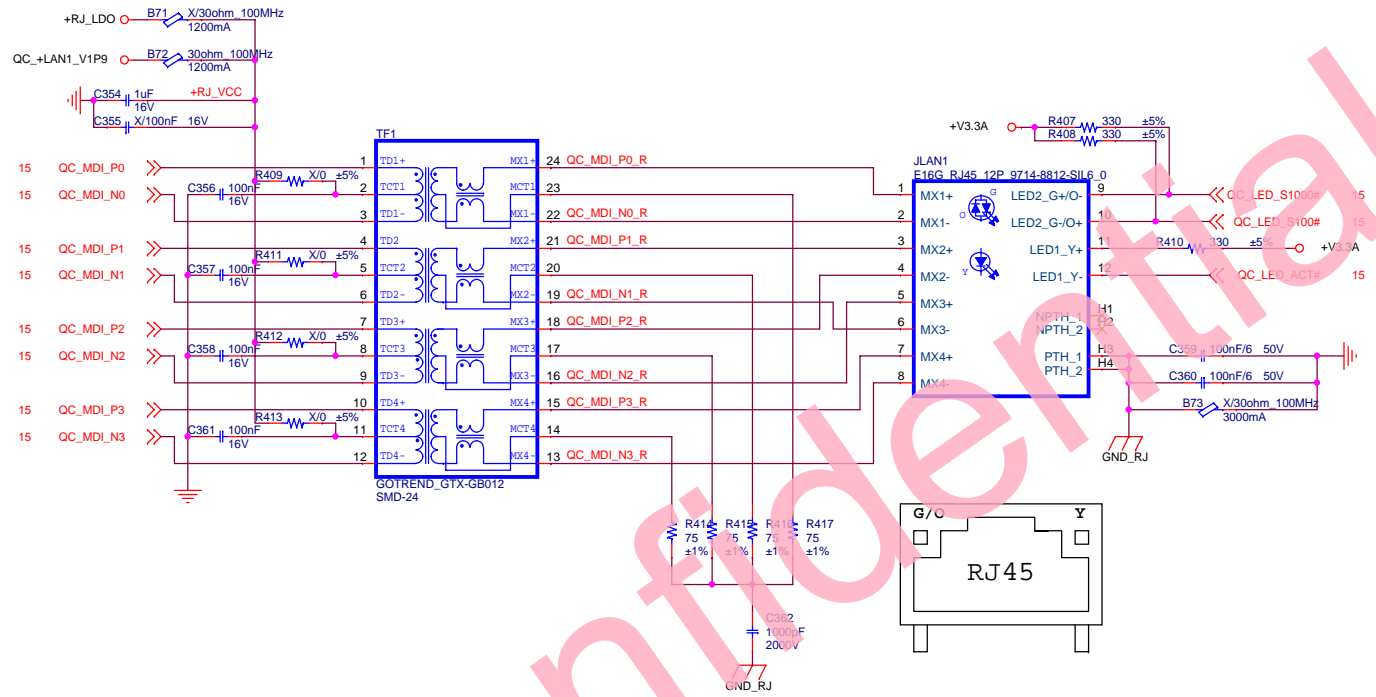
Trace width 20mils



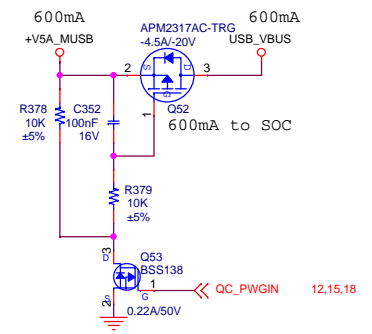
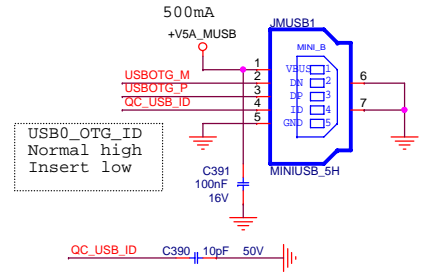
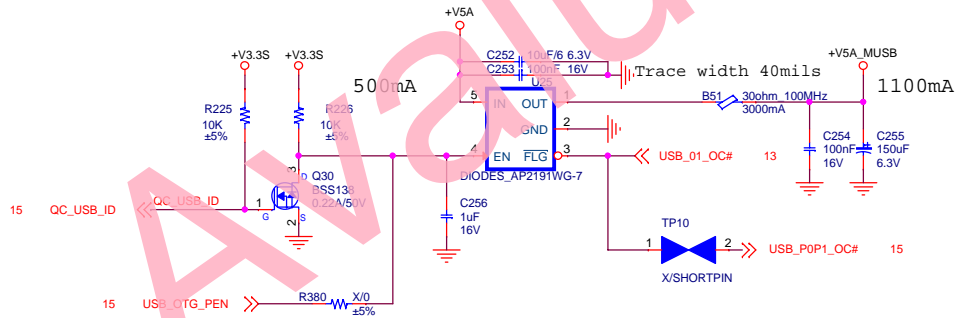
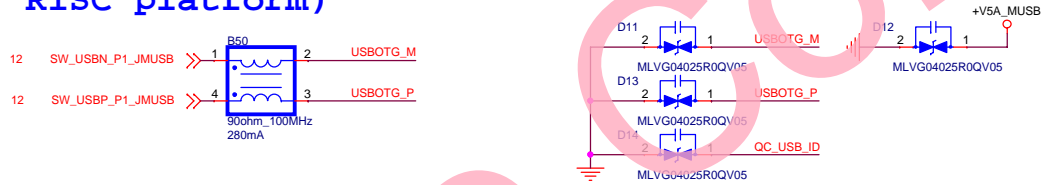
$$V_{out} = 1.2 [1 + (R_{up}/R_{dn})]$$

$$= 1.92V$$

When  $R_{up} = 6.04k$ ,  $V_{out} = 1.92V$

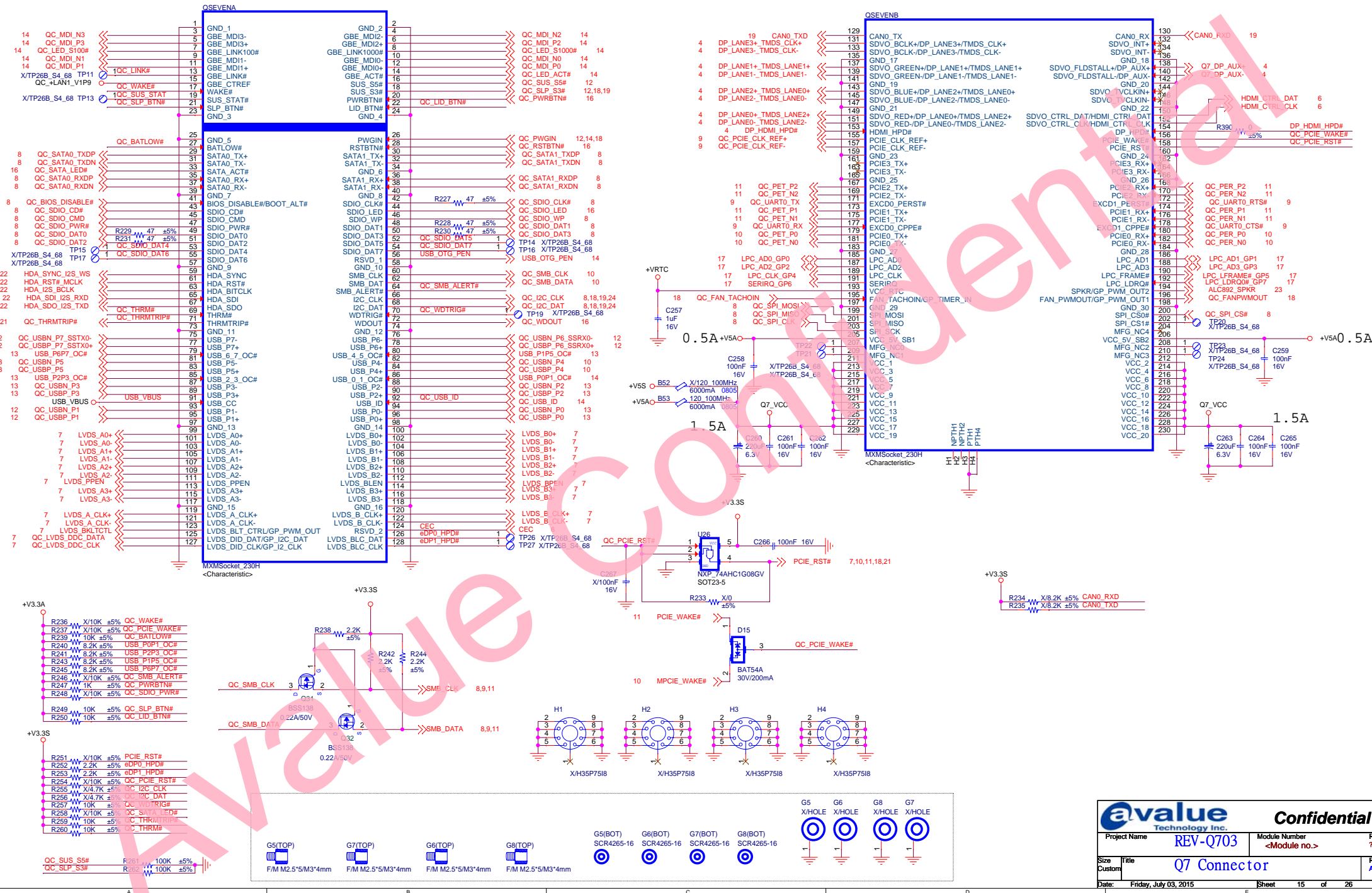


# USB OTG (For RISC platform)



<b>avalue</b> Technology Inc.		<b>Confidential</b>	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title RJ45 / Mini USB	Rev	?
Date:	Friday, July 03, 2015	Sheet	14 of 26



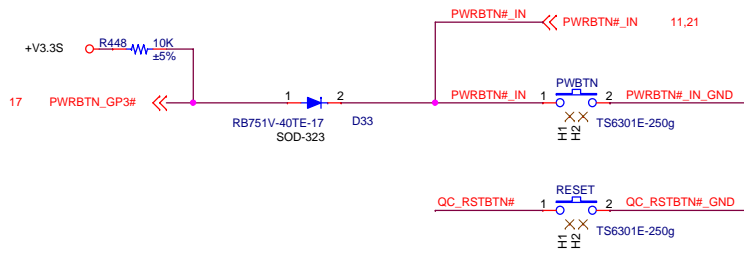
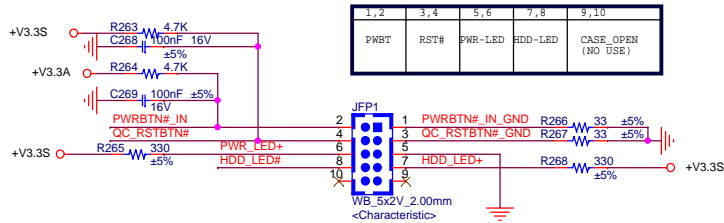


**avalue** Confidential  
Technology Inc.

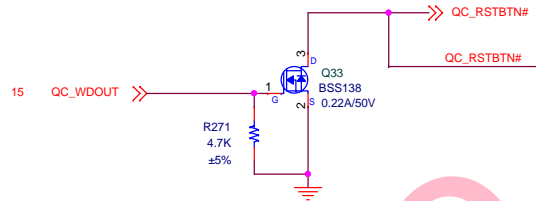
Project Name	REV-Q703	Module Number	Rev ?
		<Module no.>	
Size	Title		Rev
Custom	Q7 Connector		A1
Date:	Friday, July 03, 2015	Sheet	15 of 26



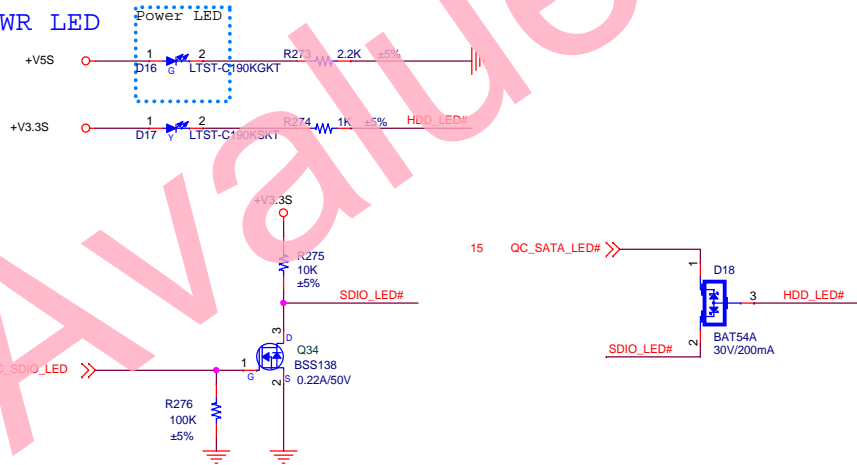
Front Panel



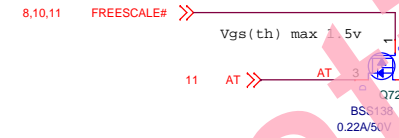
WDT



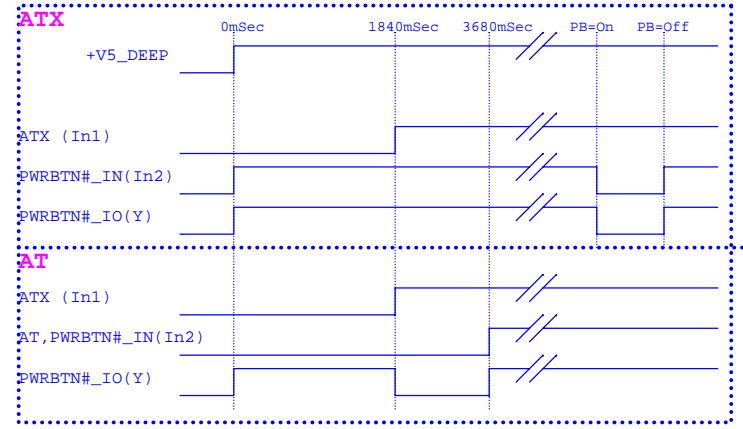
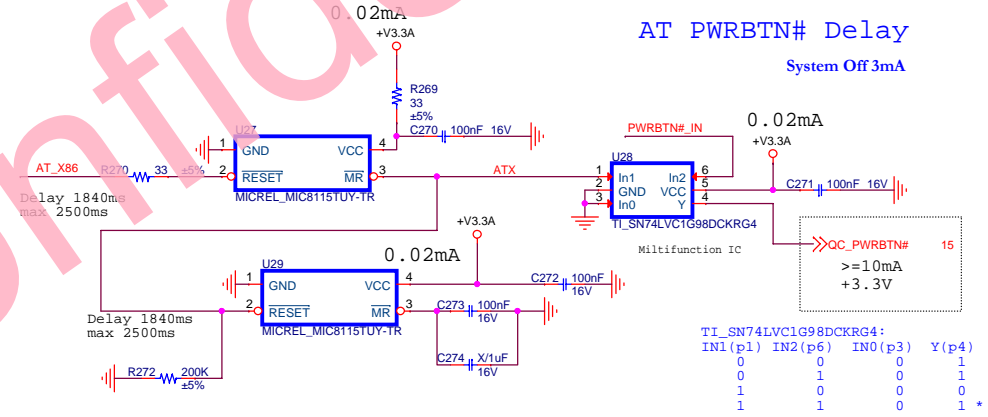
HDD LED / PWR LED

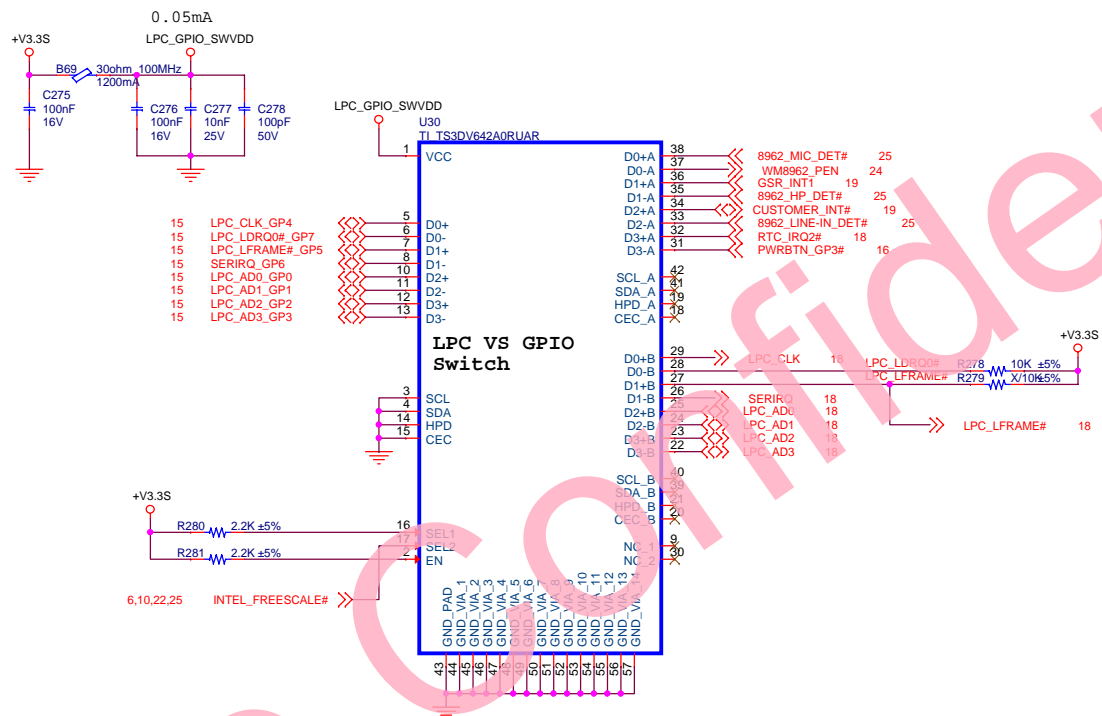


When Freescale module  
AT Mode auto power button inactive



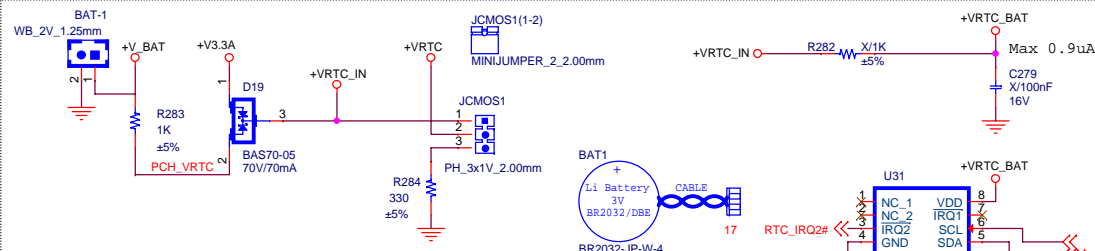
AT PWRBTN# Delay  
System Off 3mA



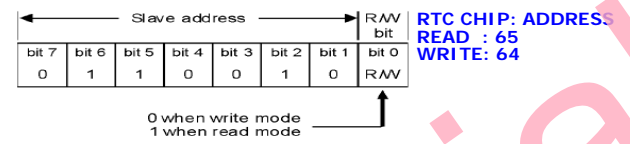


Use all channel.

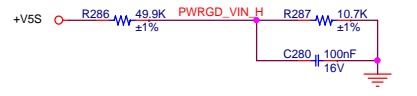
EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.



JCMOS1 SELECTION  
 SHORT 1-2 : Normal.  
 SHORT 2-3 then SHORT 1-2 : Clear CMOS.

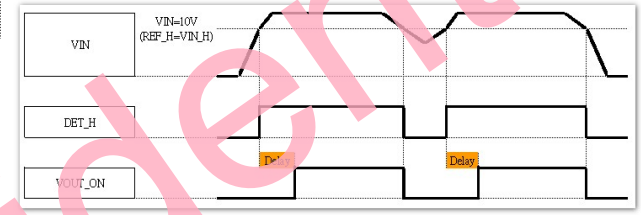
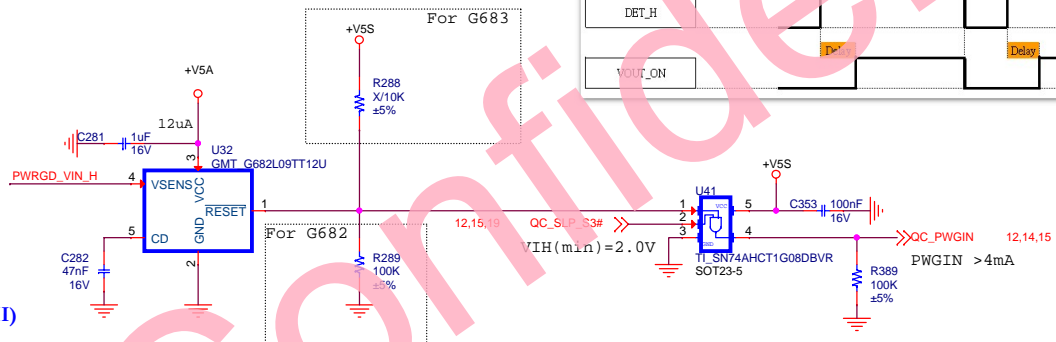


### Q7 carrier board POK

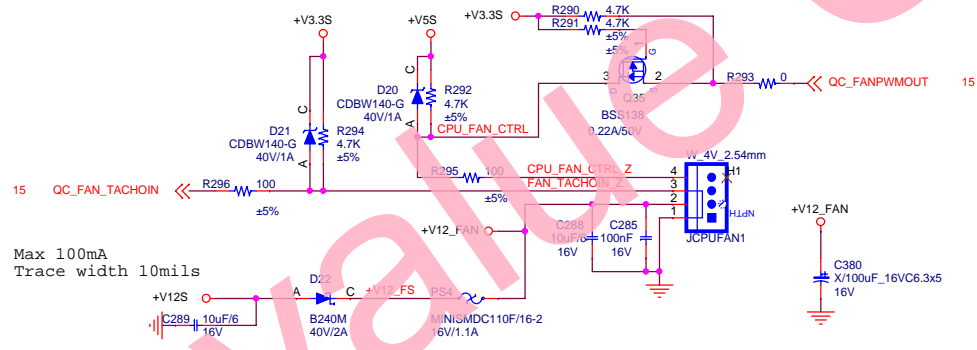


$t_{RP} \text{ (ms)} = 2.7 \times CD \text{ (nF) at } V_{CC} = 3.3V$   
 $\approx 1.27ms$

VSENS(Reset threshold 0.788V)  
 $= V_{in} \cdot R_{dn} / (R_{up} + R_{dn})$   
 $= V_{SENS} \cdot (R_{up} + R_{dn}) / R_{dn}$   
 $= 4.46V \text{ (When } +V5S\_C \text{ rising } 94.4\% \text{ output HI)}$

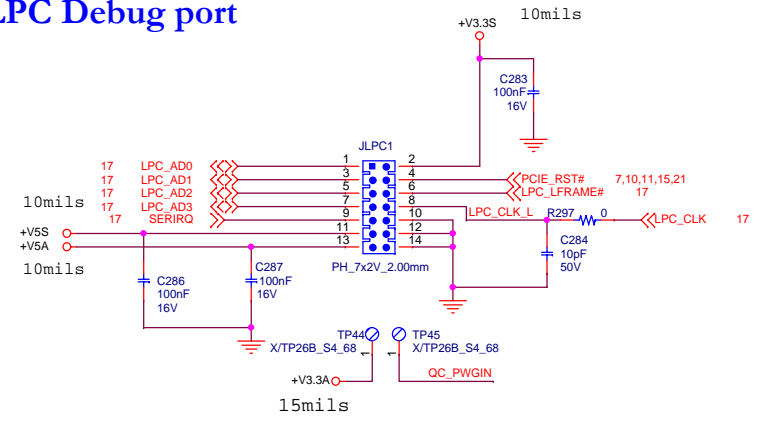


### CPU Fan

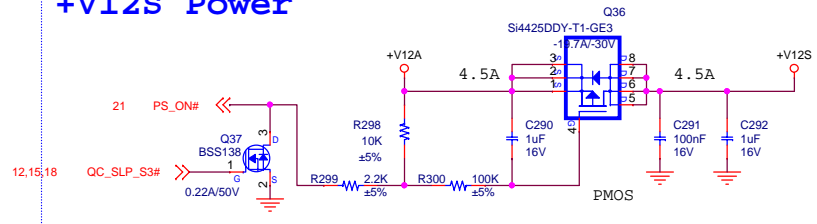


Max 100mA  
 Trace width 10mils

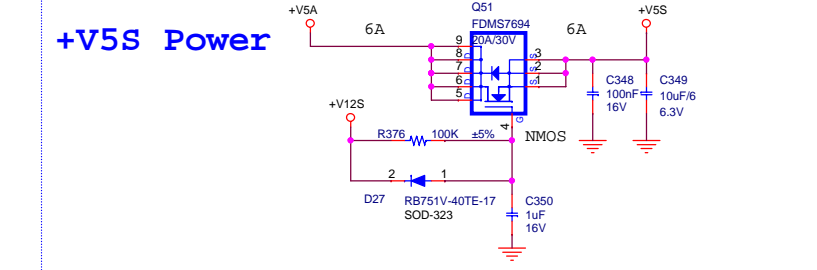
### LPC Debug port



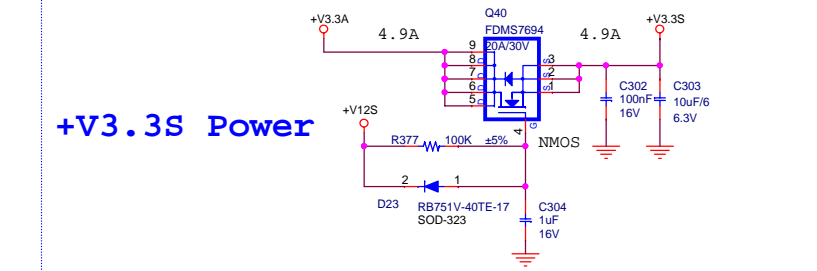
### +V12S Power



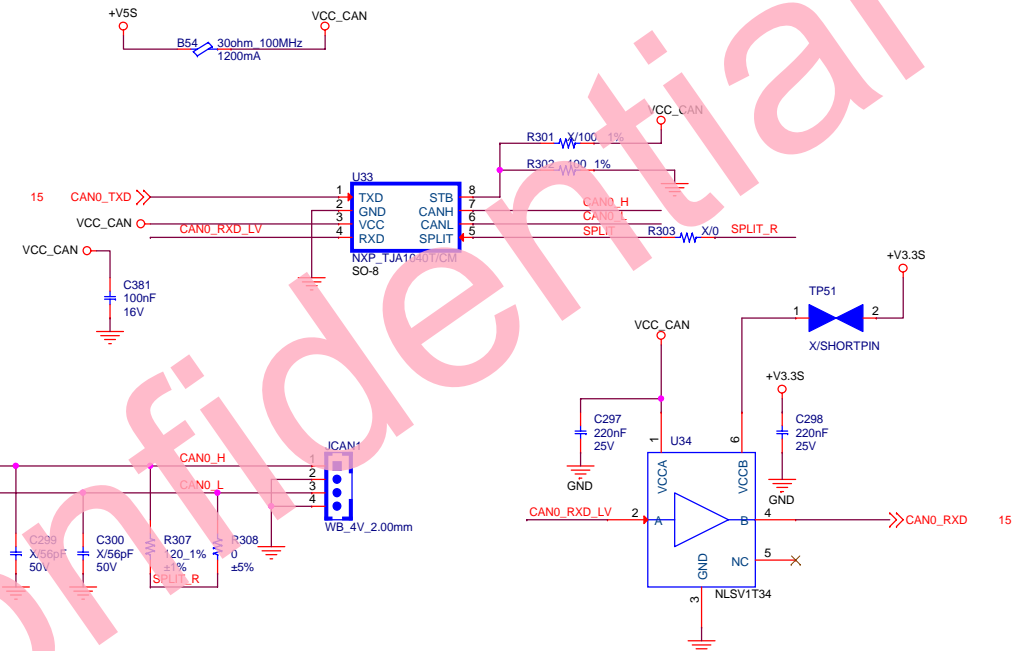
### +V5S Power



### +V3.3S Power



### CAN bus



If use SPLIT : R307 60ohm, R308 60ohm.  
If no use : R307 120ohm , R308 0ohm

### G Sensor

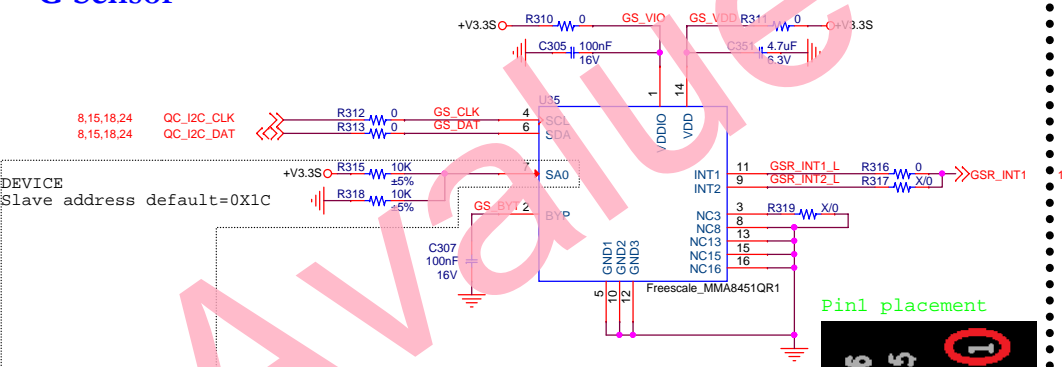
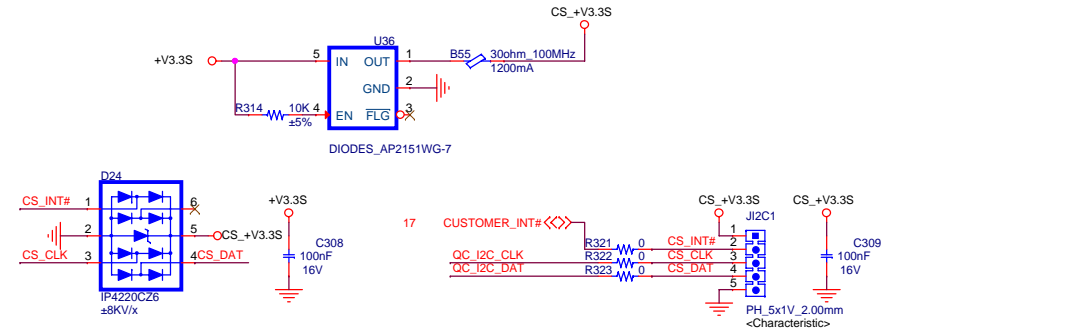


Table 10. I<sup>2</sup>C Address Selection Table

Slave Address (SA0 = 0)	Slave Address (SA0 = 1)	Comment
0011100 (0x1C)	0011101 (0x1D)	Factory Default

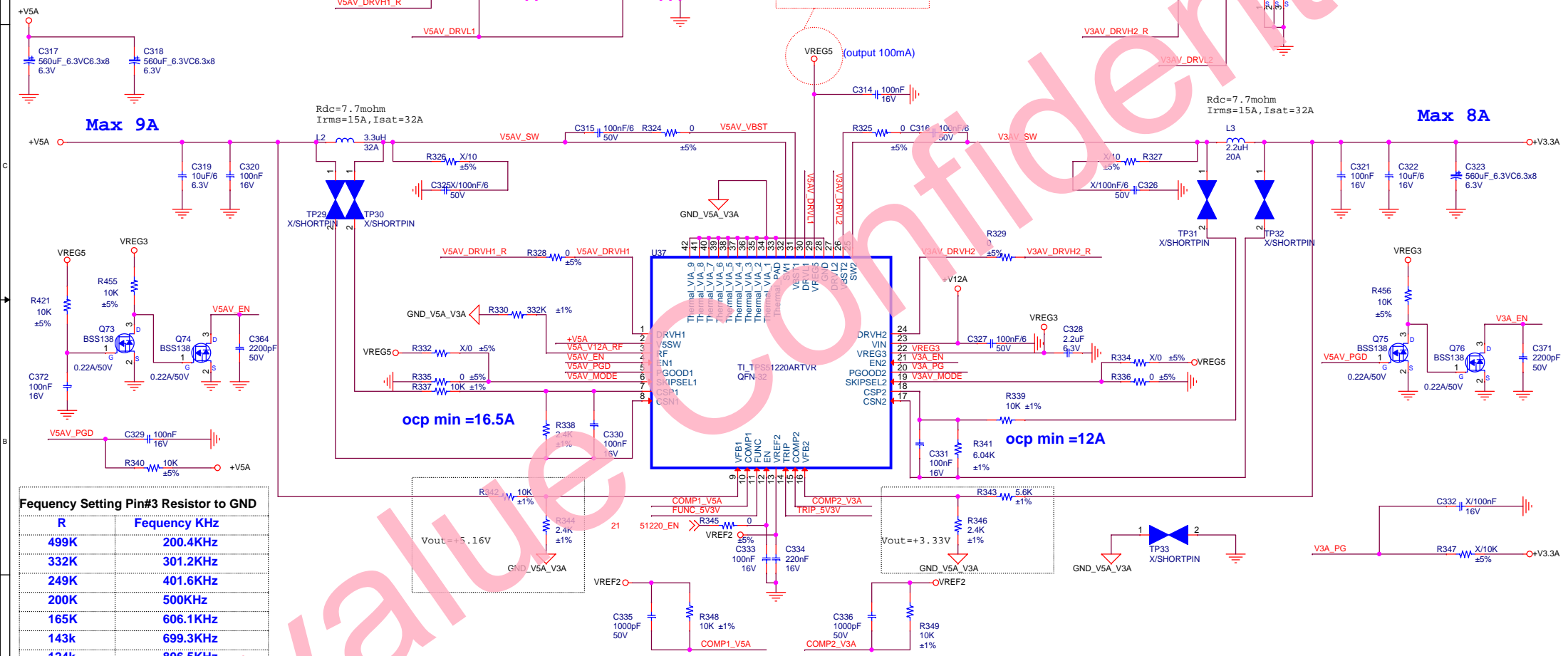
G Sensor: ADDRESS  
READ : 0X39  
WRITE : 0X38

### Customer I2C



<b>avalue</b> Technology Inc.		<b>Confidential</b>	
Project Name	REV-Q703	Module Number	<Module no.>
Size A3	Title V12S,V5S,V3.3S/G Sensor/CAN	Rev	?
Date	Friday, July 03, 2015	Sheet	19 of 26

# +V5A & +V12A Power



當PGOOD1 High時，隔了7.7ms VREG5內部的LDO會被Shut Down，改由V5SW供應5V電源。PGOOD1 Low時，會改由內部LDO Output。

ocp min =16.5A

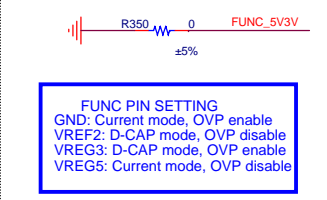
ocp min =12A

## Frequency Setting Pin#3 Resistor to GND

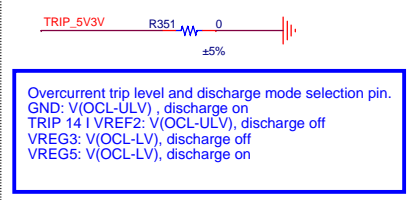
R	Frequency KHz
499K	200.4KHz
332K	301.2KHz
249K	401.6KHz
200K	500KHz
165K	606.1KHz
143k	699.3KHz
124k	806.5KHz
110K	899.1KHz
100K	1MHz

SS time Setting EN1,2 pin cap		MODE 1,2 SELECT	
X	Standard 0.96mS	GND	Continuous conduction mode
2200pF	1.1mS	VREG2	Auto Skip
3600pF	1.8mS	VREG3	Auto Skip, maximum 7 skip (suitable for FSW< 400KHz)
5600pF	2.8mS	VREG5	Auto SKIP, maximum 15 skip (suitable for equal to or greater than 400KHz)
8200pF	4.1mS		

### 12 PIN Setting



### 14 PIN Setting



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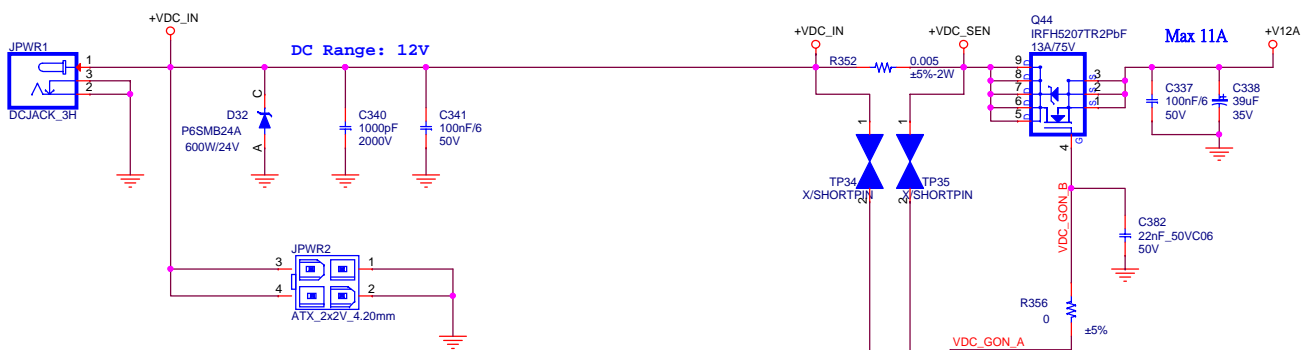
Project Name: **REV-Q703** Module Number: **<Module no.>** Rev: **?**

Size A3 Title: **TPS51220A +V5A & +V3.3A** Rev: **A1**

Date: **Friday, July 03, 2015** Sheet: **20** of **26**

# VDC-In Protection

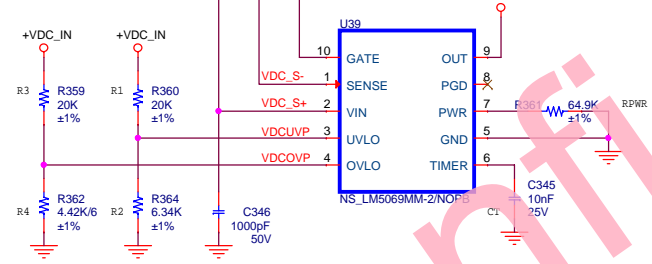
If RS = 5mohm,  
 I LIM(min) is 9.7A  
 I LIM(typ) is 11.1A  
 I LIM(max) is 12.3A



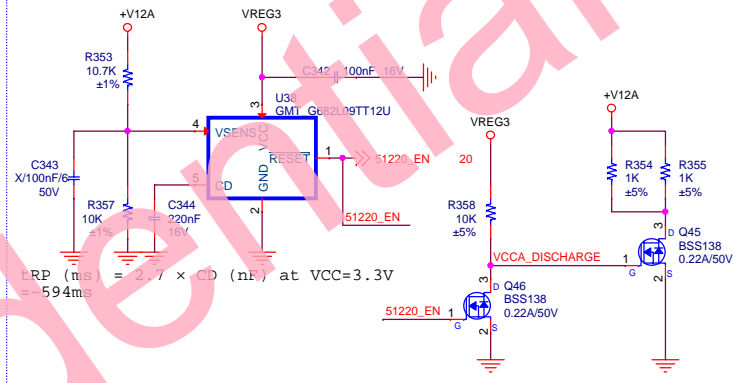
# VDC-In OVP/UV Protection

R3 = 20K, R4 = 4.75K  
 V OV is 13.25V ~ 14.36V

R1 = 20K, R2 = 5.9K,  
 V UV is 10.1V~10.59V



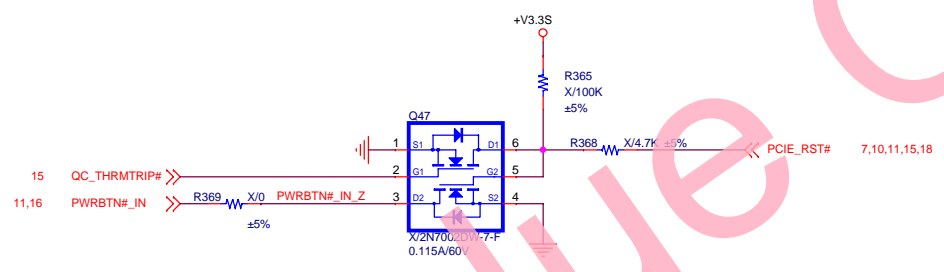
# 防瞬断放电



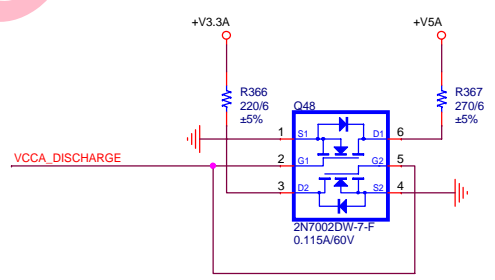
$$t_{RP} (ms) = 2.7 \times C_D (nF) \text{ at } V_{CC} = 3.3V$$

$$= 594ms$$

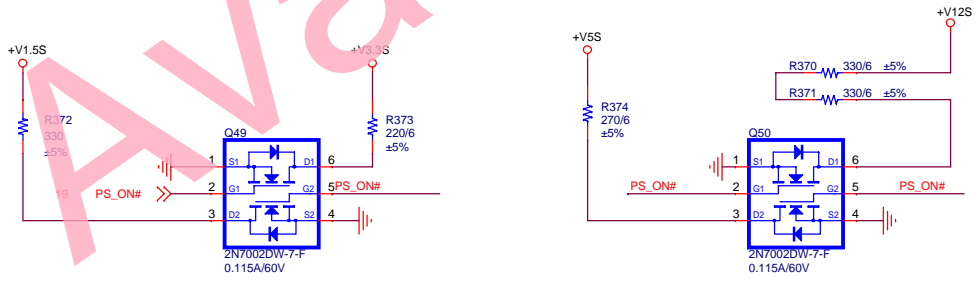
If 'THRMTrip#' goes active the system immediately transitions to the S5 State



# VCCA discharge



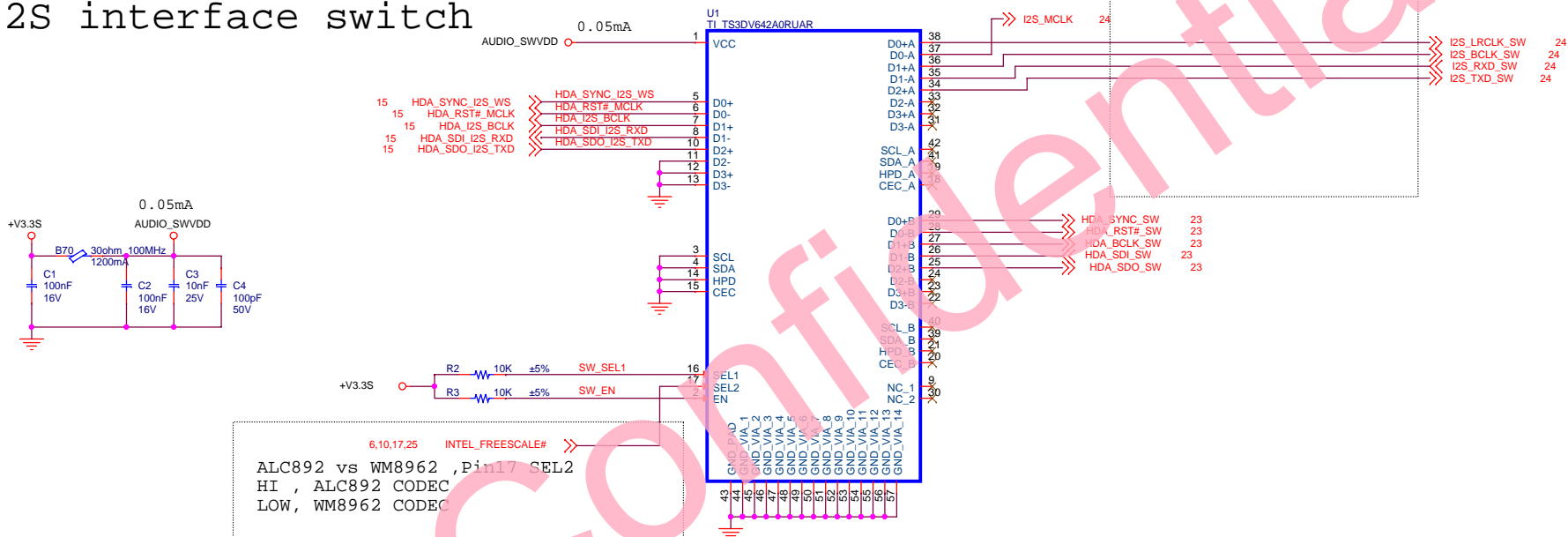
# VCC discharge



		<b>Confidential</b>	
Project Name <b>REV-Q703</b>		Module Number <b>&lt;Module no.&gt;</b>	
Title <b>DC 12 Vin / Discharge</b>		Rev <b>?</b>	
Date: <b>Friday, July 03, 2015</b>		Sheet <b>21</b> of <b>26</b>	

Del R468,Q81  
 Remove C378,C379,R467  
 Changed R26,R27,R28 from 0ohm to 22ohm.

# HDA & I2S interface switch



Don't use level shift function.  
 Direct short.

6,10,17,25 INTEL\_FREESCALE#  
 ALC892 vs WM8962 ,Pin17 SEL2  
 HI , ALC892 CODEC  
 LOW, WM8962 CODEC

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0- to D0+A/D0-A ON. All the other channels Hi-Z.
H	L	H	D0+/D0- to D0+B/D0-B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

Use all channel.

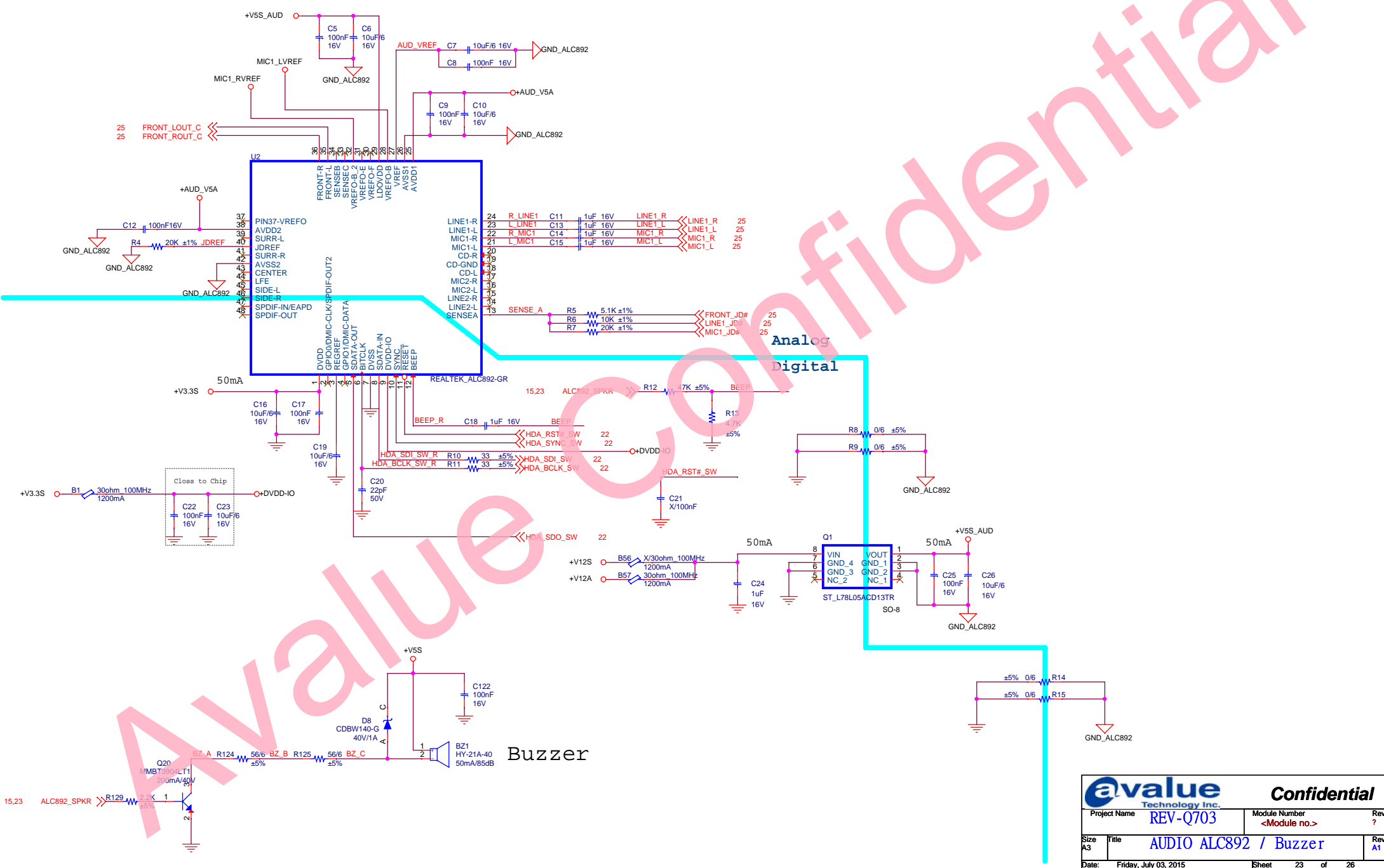
**avalue** Technology Inc. **Confidential**

Project Name: REV-Q703      Module Number: <Module no.>      Rev: ?

Size: A3      Title: HDA & I2S Switch      Rev: A1

Date: Friday, July 03, 2015      Sheet: 22 of 26





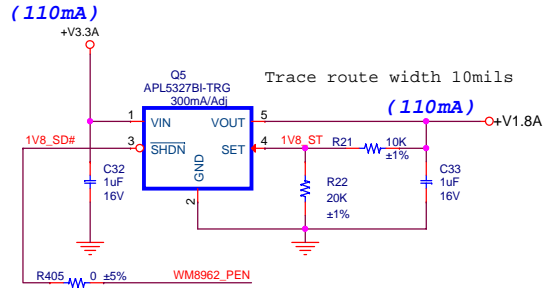
Analog  
Digital

Buzzer

		<b>Confidential</b>				
		Project Name	REV-Q703	Module Number	<Module no.>	Rev
Size	A3	Title	AUDIO ALC892 / Buzzer		Rev	A1
Date:	Friday, July 03, 2015	Sheet	23	of	26	

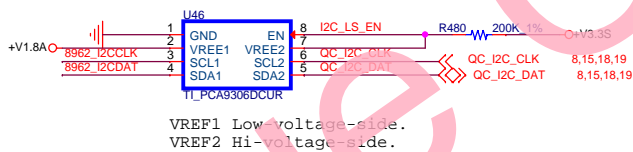
**+V1P8 POWER**

Trace route width 10mils

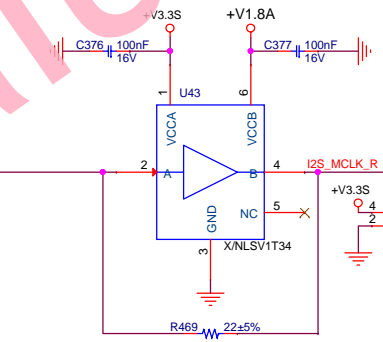


**LDO:VCC3P3 to VCC1P8 - 1.1mA**

$V_{out} = 1.2 [1 + (R_{up}/R_{dn})]$   
 $= 1.8V$   
 When  $R_{dn} = 20k$ ,  $V_{out} = 1.8V$   
 $R_{dn} = 19.1k$ ,  $V_{out} = 1.82V$   
 $R_{dn}$  recommended value is in the range of 100 to 100k.

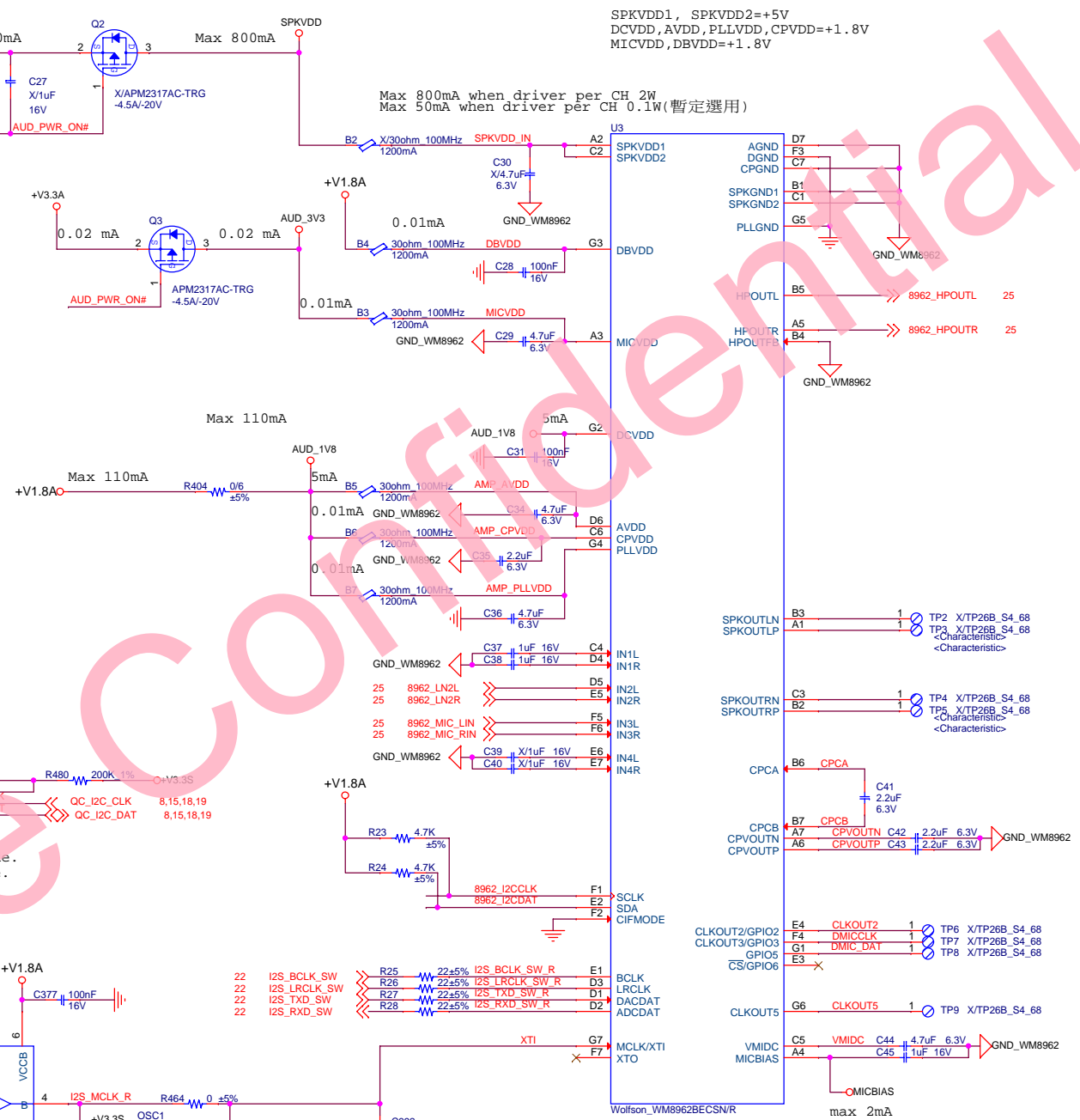


VREF1 Low-voltage-side.  
 VREF2 Hi-voltage-side.



SPKVDD1, SPKVDD2=+5V  
 DCVDD, AVDD, PLLVDD, CPVDD=+1.8V  
 MICVDD, DBVDD=+1.8V

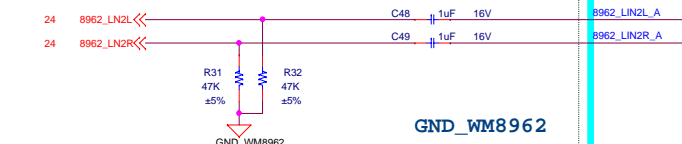
Max 800mA when driver per CH 2W  
 Max 50mA when driver per CH 0.1W(暫定選用)



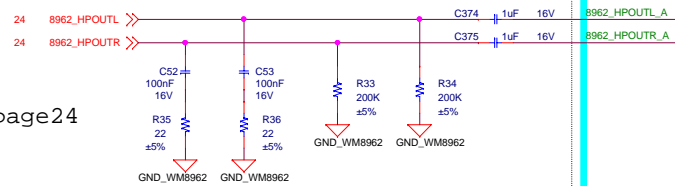
<Variant Name>

<b>avalue</b> Technology Inc.		<b>Confidential</b>	
Project Name	REV-Q703	Module Number	<Module no.>
Size	A3	Title	AUDIO WM8962
Date:	Friday, July 03, 2015	Sheet	24 of 26

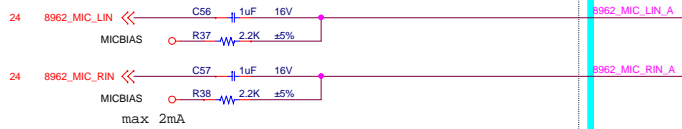
### LINE IN



### LINE OUT

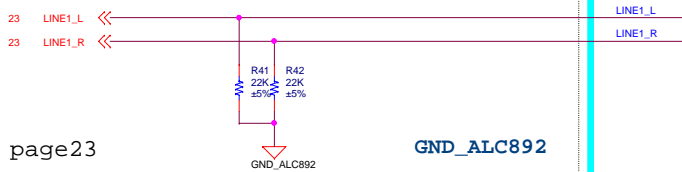


### MIC



From WM8962  
Placed on page24

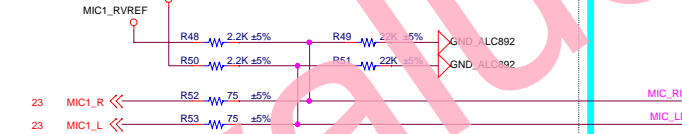
### LINE IN



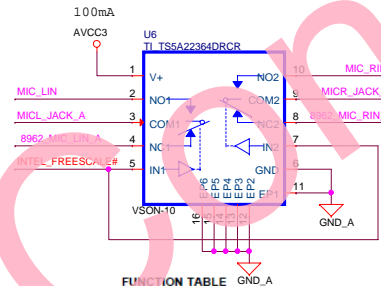
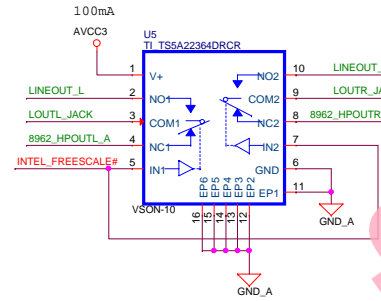
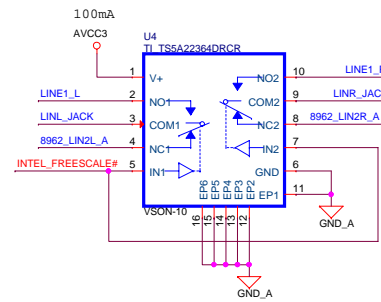
### LINE OUT



### MIC



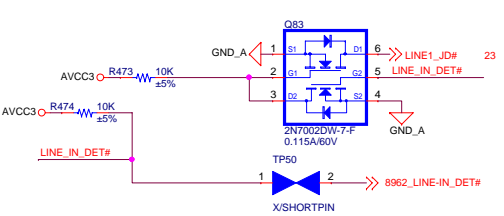
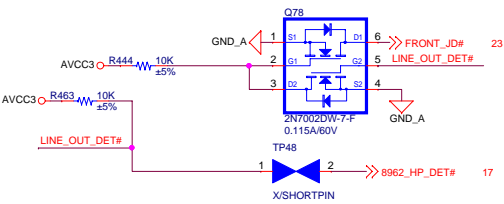
From ALC892  
Placed on page23



FUNCTION TABLE

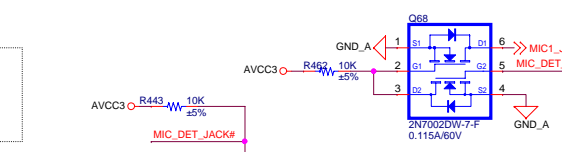
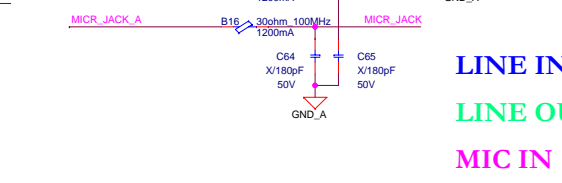
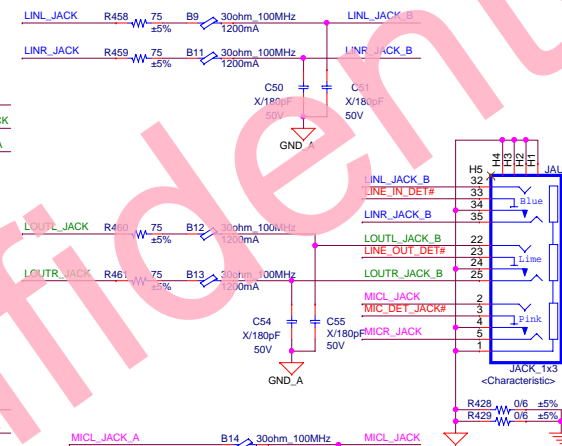
IN	MIC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

6,10,17,22 INTEL\_FREESCALE#  
ALC892 vs WM8962 ,  
HI , ALC892 CODEC  
LOW, WM8962 CODEC



$$V_{out} = 1.2 [1 + (R_{up}/R_{dn})] = 3V$$

R<sub>dn</sub> recommended value is in the range of 100 to 100k.



# Reversion History List:

REV-Q703 Ver:A0

EE :Dasmon Yang

Item	Description	Track or reason	Page	Date
0	Apply new P/N E1907Q70300RO-W1 ; E9697Q70300R ; E9695Q70300R	First Release	1	2014/09/18

REV-Q703 Ver:A0->A01

EE :Dasmon Yang

Item	Description	Track or reason	Page	Date
0	Apply new P/N E1907Q70301RO-W1 ; E9697Q70301R ; E9695Q70301R	2nd Release	1	2014/11/14
1	Add C374-C379 , R458 ~R461, Changed all luf/0603/MLCC to 0402 type.	Adjust Analog volt level	25	2014/11/14
2	Changed L1 from E121220102BH to E1212201020H.	CIS footprint error	20	2014/11/14
3	Remove R44,R45,R39,R40,R46,R47	Adjust Analog volt level	25	2014/11/24
4	Changed R352 to E10187005CXH (0.005 ohm/5%) R361 change to 64.9K_1%(E1051564921H)	Adjust Vin R sense. Setting to Mosfet Watt.	21	2014/11/26
5	R341 changed to 6.04K_1%(E1050560410H)	Setting Iccp Point	20	2014/11/26
6	Del Y1, Add OSC1 ,R457 , C373	CLOCK issue	24	2014/12/11
7	Changed C200, C347, C317, C318 and C323 to 5k hours of life cycly		20, 11	2015/1/6
8	Changed U27 to E1489811500H	At mode on/off issue	16	2015/1/7
9	Changed R287 to 10.7K/0402/1%	At mode on/off issue	18	2015/1/8
10	Add Q79, Q80, R465	SD card boot issue	8	2015/1/8
11	Changed B4 connector to +V1.8A instead of +V3.3A. Changed R33,R34 to 200k/0402.		24	2015/1/21

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EE :Dasmon Yang

Item	Description	Track or reason	Page	Date
0	Apply new P/N E1907Q70302RO-W1 ; E9697Q70302R ; E9695Q70302R	3rd Release	1	2015/4/13
1	Del R468,Q81 ; Remove C378,C379,R467 ; Changed R26,R27,R28 from 0ohm to 22ohm ; Add U46,R480	WM8962 level shift issue.	22,24	2014/11/14
2	Changed R276 from 4.7K to 100K.	HW issue	16	2014/11/14
3	Removed C388,C389,Q11,Q12 ; Add U45,R479	HW issue	6	2015/06/01
4	Add R481,R482	HW issue	9	2015/06/10
5	Del U44	HW issue	22	2015/06/29